Ultrahigh-density ‘*electrolithic’* storage memory proof-of-principle with high-aspect-ratio nanometer-sized holes

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It is estimated that more than 1 billion Tbit will be stored in the cloud in 2024 [1]. This amount has been growing at a compound annual growth rate of roughly 35% over the previous years [1]. At the same time, bit-density scaling of 3D NAND flash and hard disk drives (HDD) is becoming increasingly more difficult [2]. Therefore, it is unlikely that these two main storage technologies will remain cost-effective in the future.

To address this issue, we previously introduced ‘Electrolithic Memory’ [3], which has the potential to provide bit densities up to 1 Tbit/mm^2. This bit density significantly goes beyond the ~20 Gbit/mm^2 that 3D NAND flash reaches today [4], or even its predicted end-of-roadmap (~100 Gbit/mm^2) [2]. The ‘Electrolithic Memory’ concept relies on electrodeposition and -dissolution of multilayered metal stacks from a tight-pitched array of nanometer-sized high aspect ratio holes (Fig. 1). Provided an extremely precise control of the individual metal layer thicknesses can be achieved, these layered stacks can be used to encode information and achieve very high bit densities.

The proof-of-principle presented in [3] was limited to large area electrodes, which only allowed a few bits to be read successfully. To further understand the dissolution process that leads to a poor read-out signal, we deposited alternating Cu (10 nm) and Ni (5 nm) layers on a blanket wafer using physical vapor deposition (PVD). The resulting dense, well-defined, and uniform metal layers served as a model system for a perfectly deposited stack. As such, we can interpret the read-out signal without the uncertainties introduced by a granular or non-uniformly electrodeposited stack. By inspecting the metal stack with STEM-EDS at intermediate stages of the electro-dissolution process, it was observed that dissolution of multiple Ni|Cu bilayer occurs in three steps (Fig. 2): i) passivation of the Ni layer, ii) pinhole formation and breakthrough of that Ni layer, and iii) selective dissolution of the underlying Cu layer. This process repeats for the subsequent layers of the stack. Consequently, the dissolution leaves behind Ni residues, which obstruct read-out of layers located deeper in the stack.

Ultimately, the problem with using blanket wafers to evaluate the memory concept, is that the layers are typically thin (<100 nm) compared to the exposed coupon area (1 cm^2). Then, random pinhole formation, residue formation, and other coupon scale non-uniformities severely impact the overall read-out signal. To resolve this problem and bring the proof-of-principle closer to the final application, we fabricated patterned coupons consisting of a large array (>10^6) of holes (80 nm diameter), etched in 1 µm thick SiO_2 (Fig. 3). All the holes land on a common, blanketed Ru bottom electrode. The holes were spaced sufficiently far apart (4 µm) so that hole-to-hole diffusional crosstalk could be ignored. Using a citrate-based CuNi plating bath [5], we were now able to read out more layers, as the dissolution process occurred layer-by-layer in the nanoholes, resulting in a more pronounced read-out signal (Fig. 4).

To reach bit densities approaching 1 Tbit/mm^2, the layer thickness must be further reduced, ultimately down to 2 nm. To achieve this, the plating bath needs improvement so that dense and smooth multilayers can be obtained. In addition, despite being practical for bench-top experiments, the large array of holes must be scaled down to a single hole to provide a convincing demonstrator. Due to the small currents and charges involved for individual holes, active CMOS circuitry is necessary to amplify and control the memory hole and work is ongoing to realize such a demonstrator.

References

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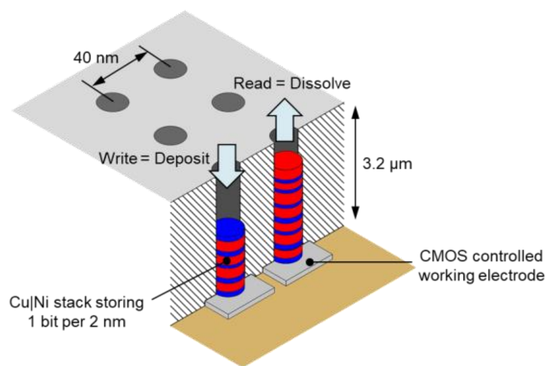

Fig. 1: Schematic of the 'Electrolithic Memory' concept, with envisioned dimensions that would lead to a bit density of 1 Tbit/mm^2.

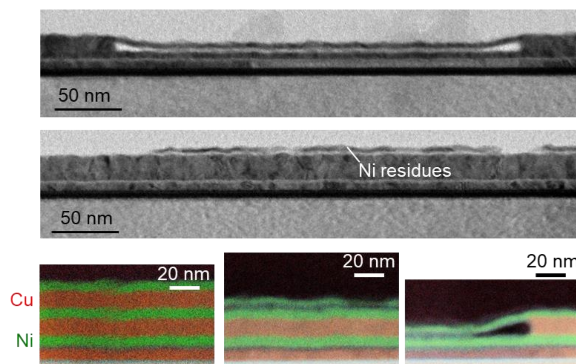

Fig. 2: STEM micrographs and EDS maps of PVD Cu|Ni stacks that have been partially dissolved electrochemically at 21 mA/cm^2 in 0.5 M H_2SO_4 (200 rpm sample holder rotation).

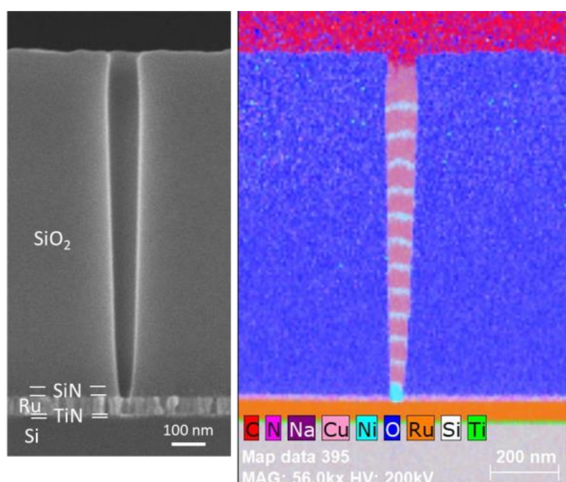

Fig. 3: (left) XSEM of a high aspect ratio hole with 80 nm diameter and 1 µm depth. (right) Electrochemically deposited $(Cu|Ni)_{12}$ multi-layered stack using a single citrate-based plating bath.

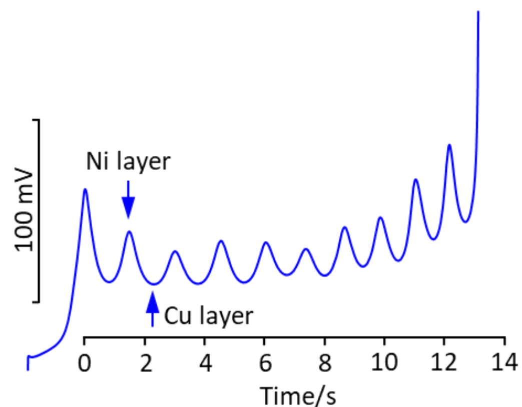

Fig. 4: Electrochemical dissolution of a $(Cu|Ni)_{11}$ multilayered stack from an array with $6{\times}10^6$ holes at 5.3 pA/hole, in the same plating bath that was used for deposition.