The role of interface chemistry and crystalline defects on the reliability of 4H-SiC MOSFETs

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The need of high efficiency energy conversion systems is expanding the silicon carbide (4H-SiC) device demand in applications with high reliability constrains (i.e. automotive etc). This imposes the scientific community to acquire a deeper comprehension of the physical phenomena affecting the device integrity under prolonged stress, with a particular focus on the impact of the crystalline defects in the semiconductor epitaxial layer. However, threshold voltage (Vth) instability phenomena and poor field effect channel mobility (μFE) are still observed in 4H-SiC MOSFETs, and can be only partially mitigated by the gate insulator post-oxidation (POA) or post-oxide deposition annealing (PDA) processes.
In this context, in this invited talk, some reliability concerns affecting the performances of 4H-SiC MOSFETs are discussed. In particular, the following aspects will be addressed: the SiO2/SiC interface chemistry and the impact of the device fabrication processes on the MOSFET threshold voltage (Vth) stability, and the impact of the semiconductor crystalline defect on the device lifetime.
4H-SiC MOSFETs were characterized by means of current voltage (ID-VG) transfer characteristics and capacitance–voltage (C-V) measurements. Furthermore, on selected failed devices, Scanning Transmission Electron Microscopy (STEM) analyses combined to electron energy loss spectroscopy (EELS), and electrical Scanning Probe Microscopy (SPM) analyses have been used to elucidate the physical mechanisms affecting their reliability. It will be shown that correlative macroscopic and microscopic (down to nanoscale) analyses are needed to fully comprehend the physical properties of the semiconductor/insulator interface and how these properties affect the real devices.
An important aspect is related the dielectric breakdown of 4H-SiC MOSFETs correlated to the presence of different crystalline defects in the 4H-SiC epitaxial layer. Of particular interest are the wafer level characterization of both the failed devices at t=0s, and of the devices showing an anomalous Fowler-Nordheim (FN) gate bias conduction. In fact, it is possible to correlate devices failing under high temperature gate bias (HTGB) stress with the presence of an anomalous FN behavior and the presence of a surface bump on the semiconductor. Moreover, the role of the threading dislocation (TD) in high temperature reverse bias (HTRB) failures was demonstrated employing high-resolution SPM techniques. These nanoscale methods elucidated the physical mechanism of the dielectric breakdown, revealing an increase of the minority carrier concentration close the insulator/semiconductor interface.
Furthermore, a method to monitor the Vth variation from single point drain current (ID) measurement using a single gate bias (Vread) value is presented. This method allowed to probe the interface states close to the 4H-SiC conduction and valence band edges and the amount of trapped charge at the interface close to 4H-SiC band edges (Nit) and inside the near interface oxide region (NIOTs).
These finding demonstrated that the threshold voltage instability of 4H-SiC MOSFETs, associated to different trapping mechanisms, is directly related to the SiO2/SiC interface chemistry and can be mitigated by an accurate control of the nitridation conditions of deposited oxides.

References

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