Selective and Self-Limited Process Technologies to Enable Ångstrom Scale Integrated Circuits

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Continued device density scaling according to Moore's Law has resulted in the adoption of 3D devices and architectures while driving critical dimensions down to atomic scales. This tutorial briefly reviews the trends in device scaling and outlines the forces driving 3D integration going forward as well as the new challenges these changes pose for future manufacturing process technologies. A look forward at the expected evolution of integrated circuit manufacturing through 3D monolithic and heterogeneous integration is presented to frame the opportunities and challenges for advanced process technologies. Selective, self-limited and atomic scale thin film process technologies that can enable 3 nm and beyond semiconductor manufacturing include plasma and thermal chemical vapor deposition (CVD), atomic layer deposition (ALD) and atomic layer etching (ALE) technologies. Selective processing including topographic and area selective deposition (ASD) is explained as an emerging technology enabling new device nodes, integration schemes and eventually the shift toward new patterning paradigms. The scope of the discussion includes examples of how these technologies enable self-aligned and sub-lithographic patterning and integration of new devices, interconnect structures and scaling boosters suitable for angstrom level process nodes. The major trends that will drive thin film innovation in semiconductor manufacturing over the next decade and beyond will also be summarized and explained.