

Multi-step Siconi pre-clean advantages for Ni(Pt)Si film formation in the frame of advanced FDSOI technology development

Magali Grégoire^a, Fabrizio Franco Morris Anak^{a,b,c}, Camille Sgrillo^a, Jean-Gabriel Mattei^a, Marc Juhel^a, and Dominique Mangelinck^b

^a STMicroelectronics, 850 Rue Jean Monnet, 38926 Crolles Cedex, France

^b IM2NP, CNRS, Aix-Marseille Université, Faculté de Saint-Jérôme, 13397 Marseille Cedex France

^c Univ. Grenoble Alpes, CEA-LETI, 38000 Grenoble, France

The demand for microcontrollers in automotive market will continue to grow in the future, and for such applications, embedded Non-Volatile Memories (eNVM) have been raised as major devices [1]. Emerging Phase Change Memories (PCM), based on HK-metal-gate 28 nm FDSOI technology (Fig.1), is one of the best candidates to achieve these challenging requirements (noted FDSOI for Fully Depleted Silicon On Isolator). For this technology, Ni-based silicide is used as contacts on active Si regions (such as gate, source, and drain), due to its low resistivity, low thermal budget, and low silicon consumption during silicide formation [2]. Nevertheless, 28 nm FDSOI technology deals with three remaining challenges: 1) ultra-thin Ni(Pt)Si film formation presenting a final thickness, around 10 nm, due to the very thin Si layer on the top of embedded oxide; 2) A specific surface preparation scheme due to the high sensitivity to Sulfuric Peroxide Mixture (SPM, as H₂SO₄ in addition of H₂O₂ solutions) chemistry of metal gate stack, formed mainly by TiN layer ([3], Fig. 2); 3) Complex Ni(Pt)Si formation in small dimensions linked to a perfect Si surface preparation to avoid any remaining oxide before NiPt deposition. For the last ten years, in-situ remote plasma clean, called Siconi, becomes the standard surface preparation process for Ni-based integrations [4]. As described in Fig. 3, Siconi pre-clean is based on two main steps, called etch and anneal steps. During the etch step, the fluorosilicate salts are generated on the wafer through the reaction of NH₄F reactive species with SiO₂ thin film in presence (Fig. 3a). The sublimation of (NH₄)₂SiF₆ salts is obtained by moving up the Si wafer near the showerhead maintained at 180 °C (Fig. 3b). Such fluorosilicate salts are quite volatile, and then transformed in SiF₄ and NH₃ gazes at 100 °C. Several previous works, mainly on TiSi advanced contacts, reported the interest for aggressive dimensions of a multistep Siconi process [5], [6]. Such process could play a role on the etching of oxide and nitride layers around gates, and then the opening of a “way” to SPM chemistry to spread up to the metal gate layer (Fig. 2). In this context, several SiCoNi pre-cleans have been investigated to improve Ni(Pt)Si thin film formation in small dimensions without damaging HK-metal gate structures. In this paper, we propose to review two separate studies performed on 300 mm blanket wafers. For the first one, complete Salicide process flow has been provided contrary to the second one for which characterizations were carried out just after NiPt layer deposition. For both, two types of SiCoNi pre-cleans have been studied as a single and multiple-step Siconi processes.

As a first result, significant reduction of Ni(Pt)Si thickness non-uniformity is measured by ellipsometry on the whole 300 mm wafer in the case of a double Siconi process, prior NiPt/TiN deposition (Fig. 4). Such improvement might be related to the fluorine species concentration at the Si surface before NiPt deposition, around 3 at. % as measured by XPS (not shown here). To clarify this point, ToF-SIMS and TEM-EELS characterizations were launched after NiPt deposition only for different Siconi pre-clean conditions. For all samples, an intermixing layer with a NiSi composition is formed at the NiPt/Si interface, and the thickness of this amorphous layer is measured by TEM near 3 nm- (Figs. 5a, b and c). Inside the intermixing layer, as shown on Figs. 5 d, e and f), fluorine distribution is very different in the case of a single-step Siconi process versus a multiple one. A double peak could be easily identified for single step process contrary to the other. In Figs. 5 g, h and i), while fluorine content is below the detection limit for EELS experiment, focusing on nickel ionization edge might enable to overcome this problem by probing nickel chemical environment such as fluorine or oxygen. EELS spectra, acquired at nickel ionization edge, fine structures indicate chemical shifts between the several layers since Ni is bonded to Pt in NiPt film, and to Si in the intermixing layer (Fig. 5a as an example). Moreover, EELS spectra exhibit the typical fine structure of Ni bonded to Pt in NiPt layer for all SiCoNi processes. Regarding the NiSi intermixing layers, EELS fine structure changes due to new bonds with Si atoms but remains the same in the NiSi layer. However, for the multiple-step SiCoNi process, EELS fine structure evidences a double peak at the interface of NiSi and Si layers (in red, in Fig. 5h). This double peak indicates a new bonding and could be related to fluorine environment. Consequently, EELS study points out a specific Ni-F binding localized at the NiSi/Si interface for the multiple-step Siconi process. Deep analyses and discussions will be then proposed in the final paper to understand which mechanisms are involved during silicide surface preparation to explain the presented results based on morphological and chemical characterizations.

References

- [1] F. Arnaud, et al., *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 24.2.1-24.2.4, 2020.
- [2] C. Lavoie et al., *Microelectron. Eng.*, vol. 70, no. 2–4, pp. 144–157, 2003.
- [3] S. Singh et al., *Solid State Phenom.*, vol. 255, pp. 105–110, 2016.
- [4] J. Lei et al., *IEEE International Symposium on Semiconductor Manufact. Conf.Proceedings*, 2006, pp. 393–396.
- [5] D. A. Ferrer et al., *Annual SEMI Advanced Semiconductor Manufact. Conf.*, ASMC, 2016, pp. 361–363 ;
- [6] M. Grégoire et al., *Micro. Nano. Eng. J.*, vol. 2, pp. 104–109, 2019.

* corresponding author e-mail: maqali.gregoire@st.com

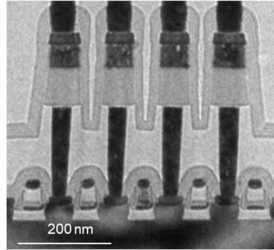


Fig. 1: TEM-cross sections of advanced low area phase change based on non-volatile memory (ePCM) realized with 28 nm FDSOI technology.

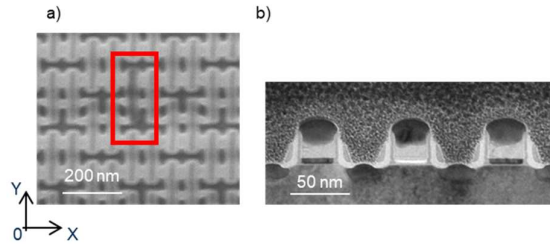


Fig. 2: Top-view SEM in SRAM arrays of a “black gate” a) defined as a TiN metal gate layer missing due to SPM chemistry etching during Ni(Pt)Si formation, as shown in b) on TEM cross-sections inside this defect.

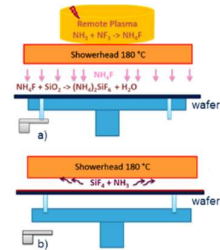


Fig. 3: Schematics of Siconi process including two main steps as $(NH_4)_2SiF_6$ salts generation (etch) a) and their sublimation (anneal) at 100 °C on the top of the wafer b).

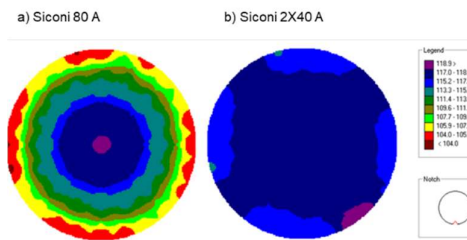


Fig. 4: Ni(Pt)Si film thickness measured by ellipsometry after RTA2 on 300 mm blanket wafers obtained after a single-step a) and multistep Siconi process b).

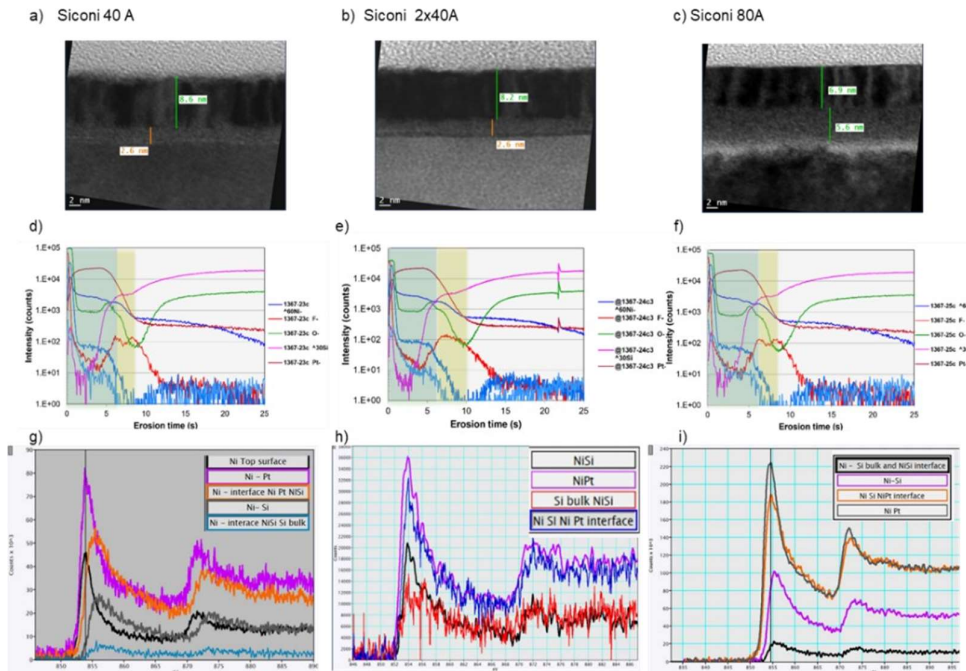


Fig. 5: TEM cross sections obtained after NiPt deposition provided after three different Siconi processes as Siconi 40 Å a), 2x40 Å b) and 80 Å c). ToF-SIMS profiles of Ni, Si, Pt, O and F elements for similar samples (d to f), and finally EELS spectra of nickel L_{2,3} ionization edge, extracted from line profiles at different regions: interfaces between the NiPt/NiSi/Si bulk and in the core of each layer (g to i).