Investigating the Evolution of Warpage Hysteresis Loop to Bifurcation Hysteresis Loop in Cu_ECD/Si large Wafers through Finite Element Analysis

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Abstract During the final thinning process, large semiconductor wafers with thick electrochemically deposited copper (Cu_ECD) layers are known to exhibit significant warpage. This warpage can manifest as either an asymmetric warpage or a bifurcation of the wafer. While finite element analysis software can predict this phenomenon, an accurate prediction requires considering the plastic behavior of the metal layer. To address this issue, a study was conducted to extend a finite element analysis multilinear kinematic hardening model of plastic Cu_ECD from a die level to the wafer level. The aim was to predict the warpage hysteresis loop and deduce the phenomenon of bifurcation during the thinning process of a 200 mm standard wafer. The results of this study have important implications for the semiconductor industry, as they offer a means of predicting and mitigating the warpage and bifurcation of large semiconductor wafers during the final thinning process.

Introduction Large semiconductor wafers, such as 200 mm nominal wafers, metalized with thick electrochemically deposited copper (Cu_ECD) layers, often experience significant warpage during the final thinning process. This warpage can degenerate into the bifurcation phenomenon, resulting in an asymmetric warpage of the wafer. While finite element analysis software [1-4] can describe the bifurcation phenomenon, accurately predicting warpage and bifurcation in large Cu_ECD metalized wafers requires consideration of the plastic behavior [5] of the metal layer. The plastic behavior of thick Cu_ECD is evident in the investigation of warpage during thermal cycling, resulting in a warpage hysteresis loop. In this investigation, we extended a finite element analysis multilinear kinematic hardening (MKH) model of plastic Cu_ECD from a die level to the wafer level to predict the warpage hysteresis loop at the wafer level and deduce the phenomenon of bifurcation during the thinning process. We tested the MKH model using experimental data reported in the literature [5] and simulated the warpage hysteresis loop at the die level of 20 µm Cu_ECD thick deposited on a Si (001) die with standard thickness. We then extended the investigation to a 200 mm standard wafer Cu_ECD metalized and compared the resulting curvatures, which were comparable. Finally, we investigated the emergence of bifurcation in thinned silicon wafer substrates.

Results

In fig.1. and 2 we report a schematic of the die and a graph of the thermal cycle utilized to simulate the warpage hysteresis loop (WHL), respectively. In fig.3 we report the comparison of the warpage resulting from the simulations and with the experimental data reported in ref [5]. In fig. 4 we investigated the upscaling of the warpage hysteresis loop by comparing the curvatures gained from the die with those gained from a 200mm wafer having both the same standard thicknesses of 730 µm. It results that the curvatures are comparable and consistent. In Fig. 5 we determined the WHL for the case of thinned wafers. As the thickness of the wafer decreases it results that the curvature increases. Moreover, by probing the resulting directional deformation at +250°C and -50°C, we can observe as the wafer bifurcates with a negative and positive curvature, respectively. In particular, in Fig. 6. we report the distribution of the directional deformation along the z-direction for the case of a wafer having a thickness of 400 µm, when the warpage hysteresis loop reaches the temperature of +250 °C. In fig. 7 we report the distribution of the directional deformation along the z-direction for the case of the same wafer, when the warpage hysteresis loop reaches the temperature of -50 °C.

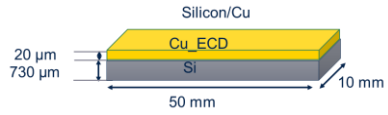

Fig.1. Schematic of a silicon (001) 5cm x 1cm die sample, 730 µm thick metalized with a 20 µm thick copper electrochemically deposited (ECD) layer.

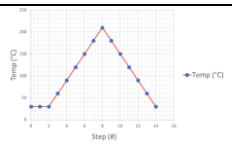

Fig. 2. Thermal Cycle exploited to simulate the plastic behavior of Copper ECD deposited on Silicon.

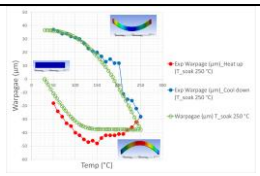

Fig. 3. Graph of the warpage hysteresis loop of a 5 cm x 1cm die Cu_ECD/Si (001) reporting the experimental data where the soak temperature was of 250 °C collected from ref [5] and the comparison with a multilinear kinematic hardening (MKH) model set up with a Ansys mechanical enterprise R2/2023.

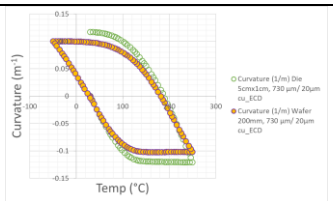

Fig. 4. Comparison of the curvatures gained from the simulated warpage hysteresis loop gained of the die of fig. 3 and that simulated for a 200 mm silicon (001) wafer having a thickness of 730 µm, according to the same MKH model.

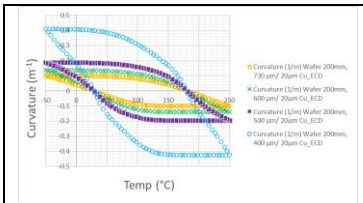

Fig. 5. Increase of the curvature of the warpage hysteresis loop of a 200 mm Si (001) wafer metallized with Cu_ECD 20 µm, modelled according to a MKH model, as the thickness of the wafer decreases from 730 µm to 400 µm.

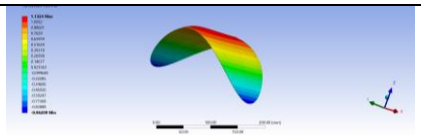

Fig. 6. Bifurcation observed at 250 °C in the warpage hysteresis loop of a 400 µm Si (001) 200 mm wafer metalized with a 20 µm Cu_ECD layer.

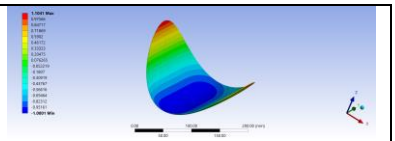

Fig. 7. Bifurcation observed at -50 °C in the warpage hysteresis loop of a 400 µm Si (001) 200 mm wafer metalized with a 20 µm Cu_ECD layer.

References

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