Parylene C as a memristive material for biocompatible memory and synaptic devices

Falk Schaller[a,*], Franz Selbmann[b], Shan Song[b], Sven Zimmermann[a], Frank Roscher[b], Stefan Schulz[a,b], Harald Kuhn[a,b]

a TU Chemnitz, Center for Microtechnologies, Reichenhainer Straße 70, Chemnitz, 09126, Germany
b Fraunhofer ENAS, Technologie-Campus 3, Chemnitz, 09126, Germany

Even though established von Neumann architectures are extremely powerful and state of the art for the current computer generation, they are not suitable for upscaling and the realization of the next computer generation. To enable future technologies such as artificial intelligence, particularly they lack of parallel data processing as well as they feature low integration densities and a high-power consumption. Hence, new approaches of computing architectures are required for the future. Doing so, neuromorphic computing based on memristive devices seems promising in order to avoid the shortages given above. Furthermore, they are suitable for the data processing on site, i.e. edge computing, as well as the data processing based on memory devices, i.e. in-memory-computing. Considering these features in combination with their low energy consumption, neuromorphic architectures can be used for wearables as well as medical implants. However, for these applications the usage of only biocompatible materials is essential. Additionally with respect to wearables, flexibility of the material is crucial.

Parylene is a family of thermoplastic polymers with a unique combination of excellent properties. These include biostability and biocompatibility according to ISO 10993, dieletric properties, low permeabilities for gases and water vapor, mechanical stability and bendability even at low thicknesses, optical transparency as well as chemical inertness against all common acids, bases and solvents. Particularly the latter enables the compatibility of parylene with established micromachining technologies. Parylene is deposited by chemical vapor deposition (CVD) according to the Gorham process, which includes the polymerization at room temperature. Hence, the deposited are free of any intrinsic stresses. Considering the given properties, parylene can be used as a barrier layer for encapsulation, as a dielectric layer for electrical insulation as well as an ultra-thin freestanding substrate for flexible electronics. [1;2]

Besides these three functionalities, the aim of the presented research was to investigate, whether parylene can be used as a memristive material to establish a fourth functionality. Doing so, memristive test architectures, i.e. metal-insulator-metal (MIM) stacks, were fabricated on 200 mm silicon wafers (Fig. 1). In a first step, silicon dioxide was thermally grown for isolation, followed by subsequent sputtering of titanium nitride as a diffusion barrier. Next, platinum electrodes with a titanium adhesion promoter were sputtered. The parylene C was deposited by chemical vapor deposition with thicknesses of 60 nm, 125 nm, 250 nm and 500 nm, respectively. Finally, the top electrode was realized by sputtering copper for electrochemical metallization (ECM), followed by platinum and aluminum for reliable probing. All three top layers were deposited using a silicon shadow mask with square openings of 100 µm², 150 µm², 250 µm², 400 µm², 600 µm², 1000 µm², 2000 µm² and 3000 µm², respectively. For characterization, the current-voltage-dependencies for all structures were measured using a wafer prober.

A typical current-voltage-dependency is depicted in Fig. 2. In summary, for parylene thicknesses of 60 nm, the growth of filaments could be easily initiated by the application of a voltage. For the different sizes given above, no area dependency was observed. Hence, it can be concluded that the mechanism is based on mono filaments. For parylene thicknesses of 125 nm, initially no growth of filaments could be stimulated. However, after three months storage at ambient temperature, memristive behavior was observed though. Thus, it can be concluded that the filaments were induced by diffusion of the copper electrode. At higher thickness of parylene, i.e. for 250 nm and 500 nm parylene thickness, only capacitive behavior was observed. In conclusion, the optimal parylene thickness is expected to be between 60 nm and 125 nm. As can be seen in Fig. 2, the hysteresis loops are comparably small, however, they are quite stable and feature a good reproducibility. Furthermore, the voltages and currents are comparably low, which makes the parylene memristor technology attractive for low-power applications. The presented research paves the way for establishing parylene as a memristive material and hence, neuromorphic computing on ultra-thin, flexible devices.
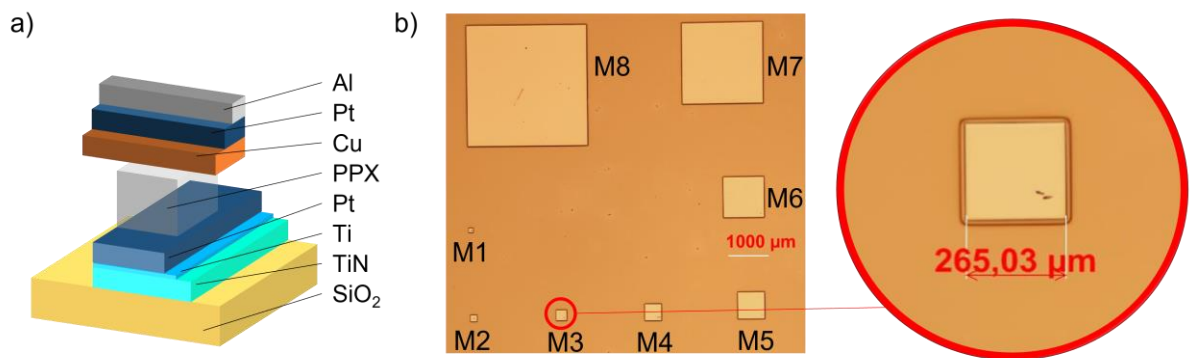
Figure 1: a) Layer structure of the memristive parylene device and b) microscopic image of a reticle with different memristor sizes (M1 - M8).
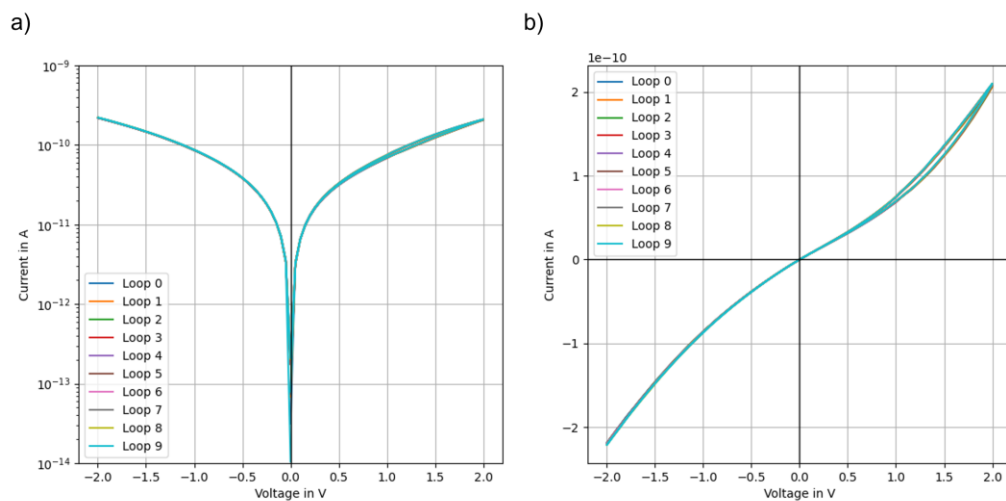

Figure 2: Ten hysteresis loops of a M3 parylene memristor with 60 nm parylene thickness and with currents in the picoampere range in a) logarithmic and b) linear scale.

References
1. F. Selbmann, C. Scherf, J. Langenickel, F. Roscher, M. Wiemer, H. Kuhn, Y. Joseph, Polym. **14**, 5246 (2022).
2. F. Selbmann, F. Roscher, F. d. S. Tortato, M. Wiemer, T. Otto, Y. Joseph, Smart Systems Integration Conf., online (2021)

* corresponding author e-mail: *falk.schaller@zfm.tu-chemnitz.de*