Local substrate removal enabling next generation fully vertical GaN-on-Si power devices

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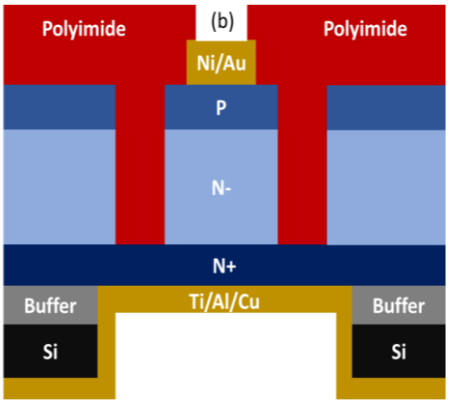
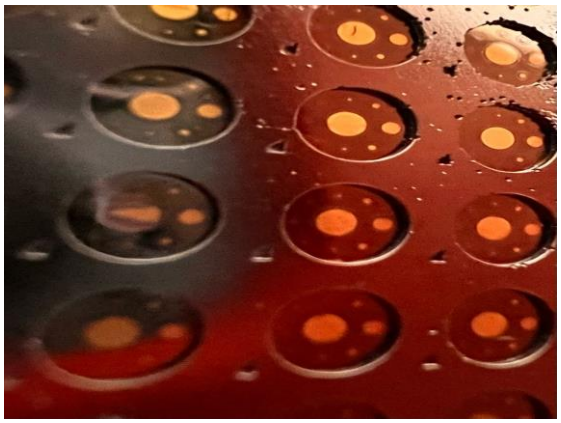
Although qualified up to 650 V voltage operation, lateral GaN devices are subject to severe limitations for higher voltage applications such as a large device size, surface trap related reliability concerns or the absence of avalanche breakdown due to the peak electric field at the gate vicinity. This led to the vertical GaN development, which is under extensive investigations worldwide as all the above-mentioned issues could be cured. State-of-the-art vertical GaN devices are fabricated on bulk GaN substrates, thanks to the high quality of the substrates in terms of low dislocation density and low impurity concentrations. However, they are prohibitively expensive, and only rather small area substrates are available.
In this talk, we will describe the current status of GaN-based fully vertical devices grown on large diameter silicon substrate. Despite the common belief about the limited drift layer thickness or wafer diameter due to the large mismatch in coefficient of thermal expansion (CTE) between Si and GaN, we will show that a local substrate removal with suitable related growth and process optimization enabled outstanding initial achievements such as extremely low on-resistance in kV-class fully vertical pn diodes with avalanche breakdown capability [1,2].



Schematic cross section of fully vertical GaN-on-Si pn diodes.



Backside view of pn diodes after Si and buffer removal

References

1. I. Abid et al, Proc. of Int. conf. on Nitride semiconductor ICNS, Japan (2023)
2. Y. Hamdaoui, Applied Phys. express **17**, 016503 (2024).

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