Direct Metal Etch and Semi-Damascene Integration of Ruthenium: A Game-changer for interconnects

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Alternative materials and integration processes as a replacement for Cu Dual Damascene have long been under scrutiny within the interconnect research communities. Reducing resistance and capacitance stands as a pivotal challenge in enhancing interconnect performance for forthcoming technology nodes. Ruthenium (Ru) emerges as a resilient contender at the metal level, diverging from Cu, owing to its resistance to oxidation, elevated melting point, low bulk resistivity [1], and the absence of a necessary metal barrier. Additionally, Ru facilitates subtractive metal semi-damascene (Fig.1) with notable integration advantages: (1) direct metal etch enables high aspect ratio (AR) patterning (Fig.2). This alleviates the constraints associated with trench filling, permitting resistance reductions at equivalent metal pitch (MP) [2,3] (Fig.3). (2) This methodology affords precise control over the height of patterned lines by adjusting the thickness of the deposited metal and the etch process, removing the need for a metal CMP [4,5]. (3) Below 22nm MP, a fully self-aligned via (Fig.4) becomes imperative to prevent via-to-line leakage [6,7].

This proposed scheme utilizes a semi-damascene integration sequence: the first metal layer is formed through subtractive metal etching. Subsequently, a highly selective etching process is employed to construct the via on top of a lower metal line by removing its hard mask (HM). The next metal level is then established using subtractive metal etching. A pioneering demonstration of 2-metal level (2ML) devices using subtractive metal etch with Fully Self-Aligned Via (FSAV) was presented by Murdoch et al. [8] (Fig.5). Subsequent enhancements in etch and cleaning procedures laid the groundwork for the subsequent implementation FSAV high yielding [9]. In this presentation, we will delve into the intricate details of utilizing subtractive patterning with Ruthenium to implement the semi-damascene scheme—an innovative approach recommended by imec as a viable alternative to Copper (Cu) damascene in advanced logic nodes.

References

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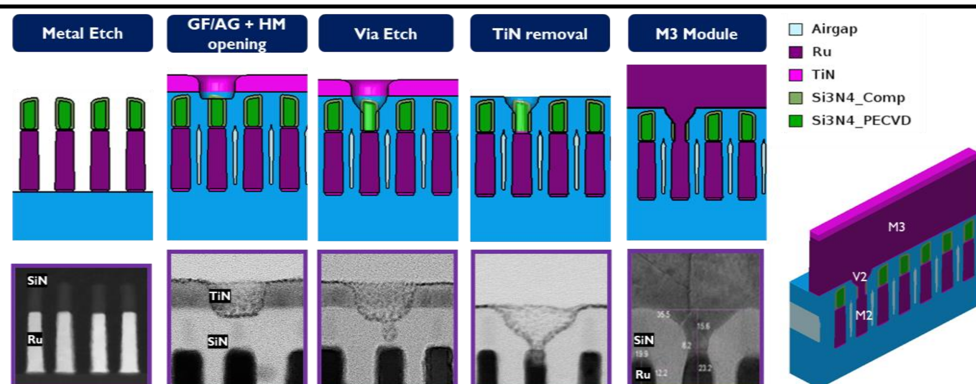

Fig. 1: Integration scheme for semi-damascene 2ML FSAV.[9]

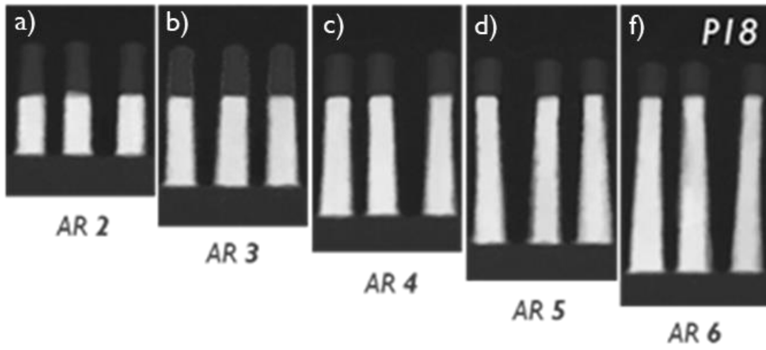

Fig. 2: a) Cross-section TEM of MP18 Ru lines with various AR (a) 2, (b) 3, (c) 4, (d) 5 and (f) 6, demonstrating a nearly vertical profile of the Ru lines and the scalability of current scheme towards higher AR. [2]

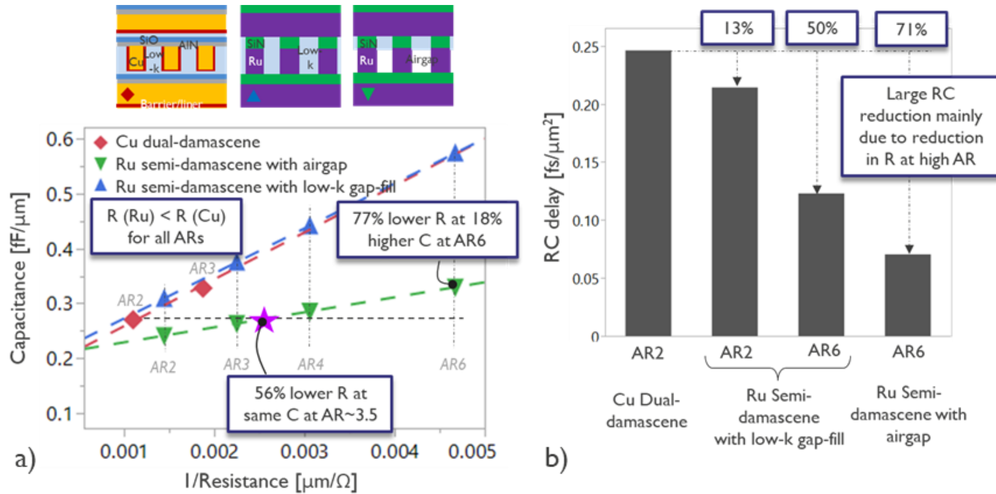

Fig. 3 3-metal-level TCAD evaluation comparing Cu-dual damascene (DD) vs Ru-Semi-damascene (SD). (a) Compared to AR2 Cu-DD, AR2 Ru-SD with airgap offers a significant, 24% lower C, while AR6 Ru-SD with airgap have comparable C. (b) RC delay product shows 13% lower RC with Ru semi-damascene thanks to lower film resistivity and barrierless Ru compared to Cu with 2 nm barrier/liner. Possibility to fabricate high aspect ratio Ru lines with airgaps in semi-damascene can lower the RC further by 71%. TCAD evaluation is carried out using imec resistivity model [9] on 10 nm width and MP18 nm 3-metal configuration as shown in the schematics.[3]

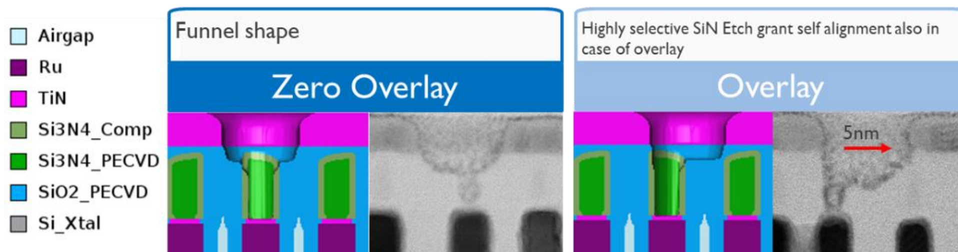

Fig. 4: Fully self-aligned model and cross-section TEM in case of zero x-shift and 5nm x-shift.[9]

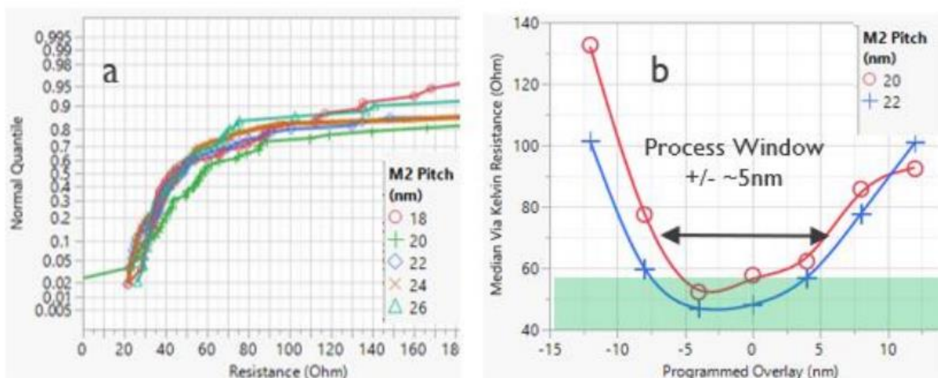

Fig 5 a) Via Resistance from 18-26nm MP and b) median via resistance vs programmed overlay for MP20 and 22nm.[8]