Ohmic contact deposition on InGaAs/InP for Si-CMOS compatible HBT fabrication

Antoine Lombrez[a,*], Nicolas Coudurier[b], Hervé Boutry[b], Alexis Divay[b], Léo Colas[b], Maël Robin[b], Stéphane Altazin[b], Thierry Baron[a]

[a] *Univ. Grenoble Alpes, CNRS, CEA/LETI-Minatec, Grenoble INP, LTM, Grenoble 38054 France*
[b] *Univ. Grenoble Alpes, CEA, LETI, 38054 Grenoble, France*

To prevent future saturation of the 5G network, the next generation with higher bandwidth must be prepared. A frequency spectrum extending up to 300 GHz has been identified as usable for 6G. Power amplification operating at these high frequencies will be necessary in future systems or Front-End-Modules. Technologies based on InP would enable power amplifiers (PAs) to reach the 300 GHz range [1]. Transistors with $\mathrm{f_{max}} \geq 1\,\mathrm{THz}$ then become mandatory in the design of such PAs. HBT-InP transistors are excellent candidates in this regard. The THz threshold has been surpassed in the state of the art with good voltage handling [2][3]. However, these technologies are implemented on expensive and brittle III-V substrates, available in the form of small-sized wafers, thereby limiting integration possibilities with commonly used interconnection solutions for lower-frequency systems. Development of an HBT-InP process integrated on a large-scale silicon substrate must then be considered.

Integrating InGaAs/InP stacks with dielectrics and achieving excellent ohmic contacts using Si-CMOS compatible metallizations are then challenges to overcome. For instance, specific contact resistivities as low as $\rho_c = 2{,}1 \cdot 10^{-5}\,\Omega.\mathrm{cm}^2$ and $\rho_c = 3{,}7 \cdot 10^{-6}\,\Omega.\mathrm{cm}^2$ on p^+-InGaAs have been obtained in other work [4], using respectively Ti and Ni as contact metals. Energy band diagrams of Ti/p^+-InGaAs and Ni/p^+-InGaAs contacts show that Ni is indeed expected to provide a less resistive contact (Fig. 1). However, lower values ($\rho_c \leq 10^{-8}\,\Omega.\mathrm{cm}^2$) are necessary for the emitter, base and collector contacts of the HBT-InP to obtain frequency performance beyond THz. Additional studies aiming to characterize and improve Si-CMOS compatible ohmic contacts have therefore been considered.

TLM structures with 100x100µm contacts are fabricated on InGaAs/InP coupons (insulating substrate) via lithography and lift-off integration, using a two-level mask. Thicknesses ranging from 5nm to 20nm of Ti, Mo, W and Ni have been tested to contact n^+- and p^+-$In_{0.53}Ga_{0.47}As$. The doping concentrations are $\mathrm{N_d} = 5 \cdot 10^{19}\,\mathrm{cm}^{-3}$ and $\mathrm{N_a} = 8 \cdot 10^{19}\,\mathrm{cm}^{-3}$. A 8nm TiN capping is deposited on Ti and W, but not on Mo and Ni. Formation of the contact plots is then finalized by depositing 30nm of Ti and 200nm of Al. Measurements on as-deposited contacts and after 300°C/60s and 400°C/60s annealings under $\mathrm{N_2}$ atmosphere have been done. Typical specific contact resistivity value on p^+-InGaAs is $\rho_c = 2{,}93 \cdot 10^{-5}\,\Omega.\mathrm{cm}^2$ and is obtained with as-deposited Mo/Ti/Al (Fig. 2). Typical value on n^+-InGaAs is $\rho_c = 1{,}12 \cdot 10^{-5}\,\Omega.\mathrm{cm}^2$ with as-deposited W/TiN/Ti/Al and Ni/Ti/Al metallizations (Fig. 3).
TLM structures with much lower contact dimensions (from 350nm to 5µm) are formed on InGaAs/InP stacks integrated with dielectrics on a 200mm silicon manufacturing platform. A Ti/TiN/W/Ti/AlSi metallization is deposited to contact the n^+- or p^+-InGaAs layer, with the same doping concentrations specified earlier. Measurements have been done, but interpreting the resistivity results is not straightforward as the calculated transfer lengths turn out greater than the contact dimensions. This implies that the limits of the usual TLM interpretation are reached. A COMSOL simulation is therefore being developed to compare the electrical results obtained by TLM extraction with those obtained by simulation. Reproduction of the measurements conditions and of the InGaAs/InP stacks integration into the dielectric/silicon environment is being worked on before starting the simulations (Fig. 4).

The authors acknowledge the support by the French National Research Agency which is funding the Electronic research program (PEPR T-REX 6G). This work was partly supported by the French Renatech network.

References

1. Wang H., and al. [Online]. Available: https://gems.ece.gatech.edu/PA_survey.html
2. Urteaga, M., and al. 2016 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM). IEEE, 2016.
3. Arabhavi, Akshay M., and al. IEEE Transactions on Electron Devices 69.4 (2022): 2122-2129.
4. Boyer, Flore. PhD Thesis. Université Grenoble Alpes, 2020.

* *corresponding author e-mail: antoine.lombrez@cea.fr*

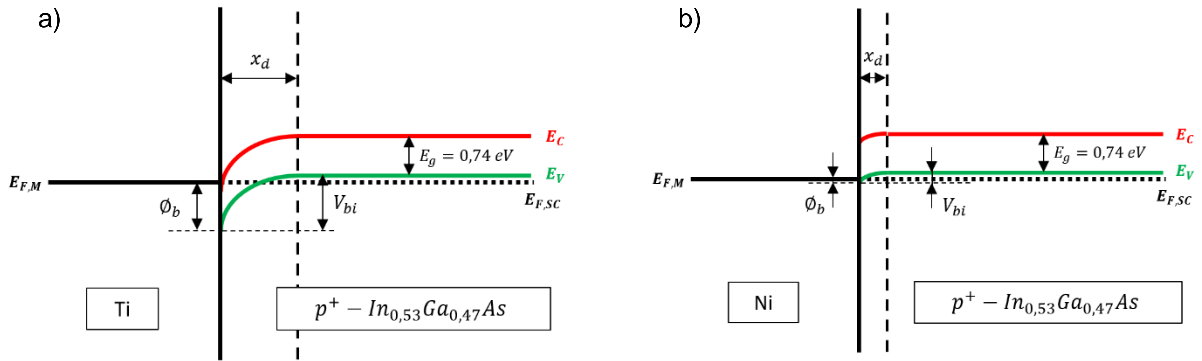

Fig. 1: Energy band diagrams of (a) Ti/p⁺-InGaAs and (b) Ni/p⁺-InGaAs contacts ($N_a = 8.10^{19}$ cm^{-3}). Fermi level pinning by surface states is not considered.

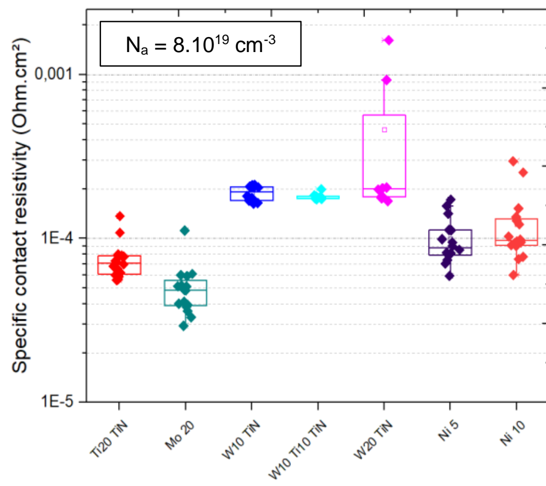

Fig. 2: Measured resistivities of as-deposited Si-CMOS compatible contacts on highly p-doped InGaAs.

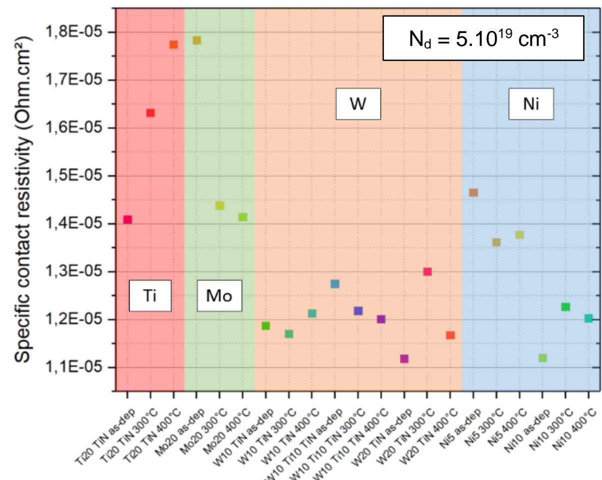

Fig. 3: Measured resistivities of as-deposited and annealed Si-CMOS compatible contacts on highly n-doped InGaAs.

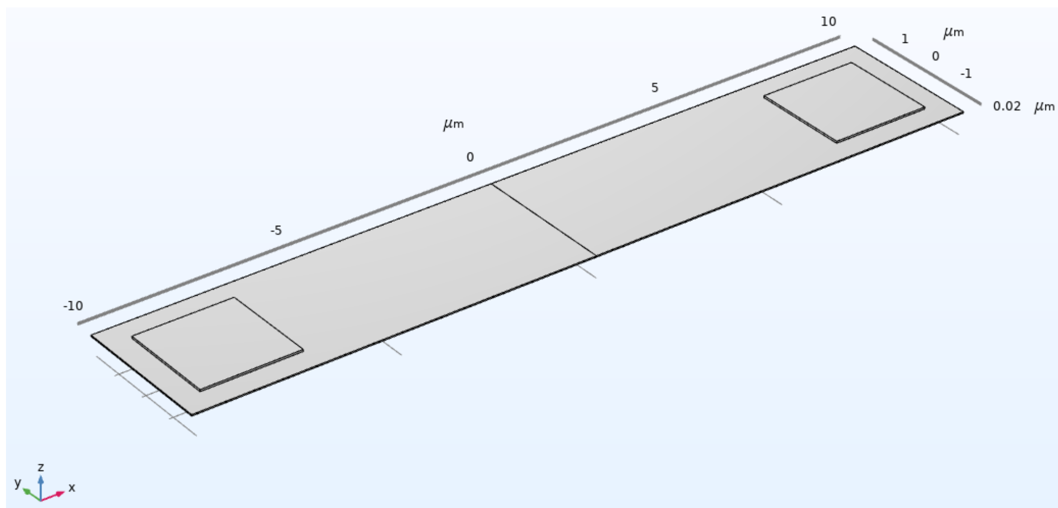

Fig. 4: Reproduction of the TLM structure geometry in COMSOL.