Development of Novel Selective Barrier Metal for Low Via Resistance in Cu Damascene

Eunji Jung, Seungyong Yoo, Chibeom Park, Seungkeun Cha, Jungmin Lee, Jungmo Yang, Eunjeong Na, Lynne Heo, Heemin Yang, Seongbeum Kim, GeunMyeong Kim, Junki Jang, DooHwan PARK, Jeong Hoon Ahn, Rak-Hwan Kim, Taehong Ha

Foundry business, Samsung Electronics Inc., Hwasung, Gyeonggi, Rep. of Korea

As the logic device node gets smaller, the impact of the resistance and capacitance (RC) time delays in the Back-End-of-Line (BEOL) interconnect becomes a significant factor in determining the performance of the chip. To minimize RC delay, it is crucial to focus on reducing the resistance in vias [1]. However, developing a barrier metal capable of maintaining barrier properties and withstanding severe stress at the bottom of vias in an extremely small metal pitch poses significant challenges. While Atomic Layer Deposition (ALD) Barrier Metal (BM) has been introduced to replace traditional Physical Vapor Deposition (PVD) BM to reduce via resistance [2], overcoming delamination issues due to stress build-up on the via bottom remains challenging, given ALD BM's impurity characteristics and stress differential from PVD BM.

This paper presents an optimized selective ALD barrier metal process designed to reduce via resistance while addressing the shortcomings of ALD BM. The selective deposition ALD process incorporates a concept where the deposition and removal process of self-assembled monolayers (SAM) is added to the existing copper (Cu) process [3-4] (Fig. 1). Before depositing the tantalum nitride (TaN) BM, SAM is selectively deposited on the exposed metal layer's surface, rather than the low-k Inter-Metal Dielectric (IMD) surface, providing hydrophobicity to prevent TaN deposition at the bottom of via during atomic layer deposition. Consequently, ALD TaN can be selectively deposited on the low-k surface, resulting in reduction of via resistance (15~20%) (Fig. 2). To achieve an effective selective deposition process, various factors such as SAM soaking time and temperature, ALD TaN thickness, plasma process for SAM removal, and physical vapor deposition conditions for densification must be considered. Optimizing SAM process conditions involves determining the deposition temperature and soaking time, ensuring SAM removal is easy. The optimal condition is derived based on the final ALD TaN film quality characteristics. The SAM removal process utilizes mild H2 plasma, selected to minimize plasma damage to IMD and meet the standard for completely removing carbon residue originated from SAM deposition (Fig. 3).

One of the most challenging issues in reducing via resistance is the reliability limitations, including stress migration and electro-migration in the copper damascene structure as the pitch decreases. Despite the trade-off between lower via resistance and reliable processes due to increased barrier metal thickness, ALD TaN barrier shows limitations in achieving better performance (Fig. 4). In this regard, selective ALD BM offers advantages in overcoming the limitations of ALD BM. This is attributed to the characteristics of Physical Vapor Deposition (PVD) Barrier Metal (BM), where even with a thinner BM thickness, maintenance at the bottom of via and improved adhesion properties at the sidewalls of via can be achieved. This advantage is evident in stress simulation results and improved health-of-line (HOL) in the wide metal stack chain Test Element Group (TEG), as depicted in Figure 5. Furthermore, excellent yield results were obtained by optimizing the subsequent PVD BM treatment process conditions (Fig. 5).

In conclusion, to reduce via resistance of the copper (Cu) interconnect, we performed process optimization for Self-Assembled Monolayers (SAM) deposition and removal conditions which are critical parameters in the selective Atomic Layer Deposition (ALD) BM process. The via resistance was successfully reduced by 20% or more. Additionally, addressing delamination and reliability issues arising from stress concentration in the tiny pitch structure is a challenging aspect of Barrier Metal (BM) scaling. However, through the optimization of selective ALD BM, these challenges can be addressed by reducing impurities at via bottom and enhancing film density at the sidewalls of the via.

References

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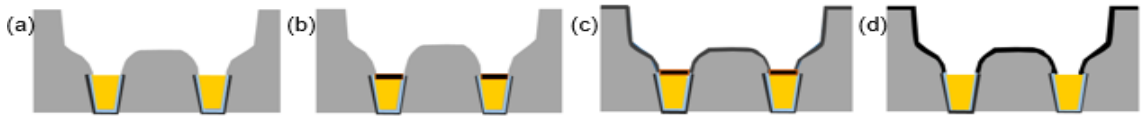

Fig. 1. Process sequence of selective ALD TaN Deposition (a) after pre-clean for interface (b) SAM deposition (c) selective ALD TaN deposition (d) SAM removal process

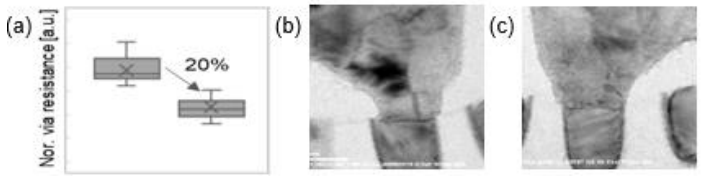

Fig. 2. (a) Via Resistance gain of selective BM (b) TEM image of ALD BM (c) TEM image of Selective BM

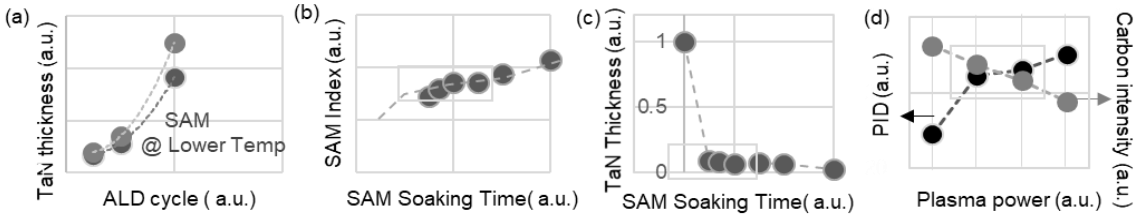

Fig. 3. Optimization of selective BM (a) SAM temp vs. TaN thickness (b) SAM soaking time vs SAM thickness (c) SAM soaking time vs. TaN thickness (d) PID (plasma induced damage for LK vs. intensity of carbon impurity by Plasma power for SAM removal

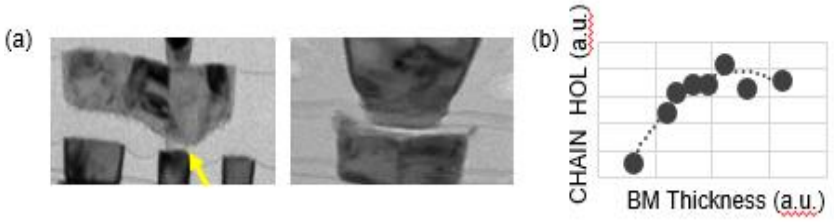

Fig. 4. (a) ALD BM delamination issue at via bottom (b) BM thickness vs. Via Chain HOL (health of line, %)

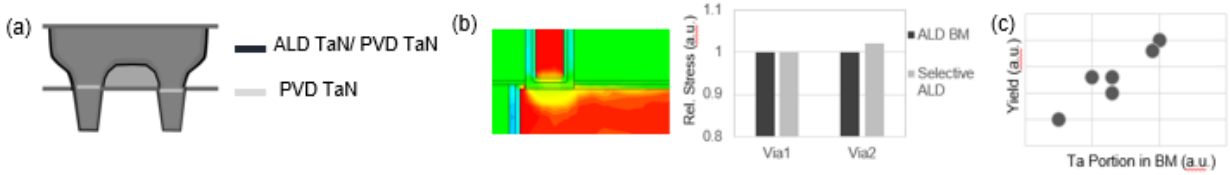

Fig. 5. (a) Selective ALD BM final BM profile: PVD BM only at via bottom (b) Stress simulation of ALD BM (c) Ta portion in BM vs. Yield