Ohmic Contact Formation and Atomic Layer Processing for Nitride Devices

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Nitride devices e.g. AlGaN/GaN heterostructures are one of the main candidates for current power electronics and RF applications [1,2]. To improve device performance materials with either higher spontaneous polarization fields to increase carrier density in the two-dimensional electron gas (2DEG) formed at the heterointerface, or with a higher band gap are investigated [3, 4]. In both cases, the formation of the ohmic contact to the 2DEG is demanding and for the smaller and smaller devices the contact resistance of source and drain becomes crucial for the resulting ON-resistance. Here, our efforts to develop material stacks to form ohmic contacts with ultra-low contact resistance to the different heterostructures will be summarized. Varying the standard approach of a Ti/Al/Ni/Au contact stack V [5] and other transition metals were used to lower the thermal budget for alloy formation and gold free stacks like V/Al/Ti/TiN [6] were investigated to enable CMOS compatibility.
On the other hand, dielectric thin films are introduced by atomic layer deposition (ALD) to lower gate leakage current and hence increase the ON/OFF ratio further in a so-called MISHEMT (metal insulator semiconductor high electron mobility transistor) device. The impact of a fully amorphous dielectric (Al_2O_3), which was kept amorphous by the integration of a low thermal budget ohmic contact [5], was compared to an epitaxial dielectric film ($GdScO_3$) [7]. Due to the band alignment and the high dielectric constant of $GdScO_3$, the spillover effect as it was seen for Al_2O_3 [8] has been suppressed, and a reduction of threshold voltage shift due to the additional capacitance by the dielectric layer has been achieved. In addition, $AlTiO_x$ films were investigated as gate dielectrics, which enable a field and band alignment engineering allowing gate leakage reduction with minimal threshold voltage shift [9].
These approaches can be combined with atomic layer etching processes (ALE) to further reduce contact resistance by a source drain recess, and shift threshold voltage towards positive bias by a gate recess [10]. In the last case, a combination with *in-situ* ALD processes allows preventing an unwanted increase of gate leakage current by the recess process.

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