Chip Package Interaction assessment of WLCSP process steps by 3D FEM Thermo-mechanical simulation

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New power technologies are increasingly moving to Wafer Level Chip Scale Package (WLCSP) solutions [1], in order to optimize electrical connections, avoid parasitic loss and reduce overall size of the product. The integration of these package families, from a Chip Package Interaction (CPI) point of view, is very different from what has been already done and known on standard plastic packages: no thermo-mechanical stress due to wire bonding and molding compound is here present. Anyway, a risk assessment of WLCSP process must be addressed to study assembly impact on passivation and top metallization morphologies, due to the temperatures used to complete all the steps.
Finite Element Method (FEM) simulation is a powerful tool for evaluating stress due to thermal and mechanical mismatch, able to highlight worst conditions for different layout configurations.
In this work, a 3D WLCSP thermo-mechanical modeling activity is presented to evaluate stress generation during assembly phase. The interconnection system considered is a fan-in WLCSP with two organic insulator layers (PI1 and PI2), one redistribution metallic layer (RDL), under bump metallization (UBM) and solder balls. All these steps, excluding soldering, are performed at wafer level in an assembly fab. The silicon technology under investigation has a top metal scheme composed by a thick Al metal covered by two dielectrics: a Silicon Oxide and a final Silicon Nitride passivation film that is the material under analysis for this stress evaluation activity. A scheme of the package and die considered system is reported in Figure *1*.
Thermo-mechanical simulations are performed using Comsol Multiphysics software by a linear elastic materials model including initial stress of some layers if applicable. Silicon Nitride has been analysed considering its risk of breakage, so the considered physical quantity is the First Principal Stress.
Firstly, passivation stress has been analysed for different process steps: a comparison of stress at wafer level before assembly (simulation of a thermal treatment), after PI1 and PI2 curing, bumping and soldering is reported. PI2 curing appears as the most critical step: the simultaneous expansion of PI1, RDL and PI2 layers generates a high stress level in SiN passivation as reported in Figure *2*. Once identified the worst process step in terms of stress, also a comparison of different layout configurations is reported, considering different cases of RDL and PI2 opening.
Finally, some considerations about passivation breakage risk highlighted by this analysis and a way to design dedicated experimental trials are reported as conclusions and important outputs of this work.

References

1. “Wafer Level Packaging (WLP): Fan-in, Fan-out and Three-Dimensional Integration”, Xuejun Fan, EuroSimE 2010 11th International Conference.

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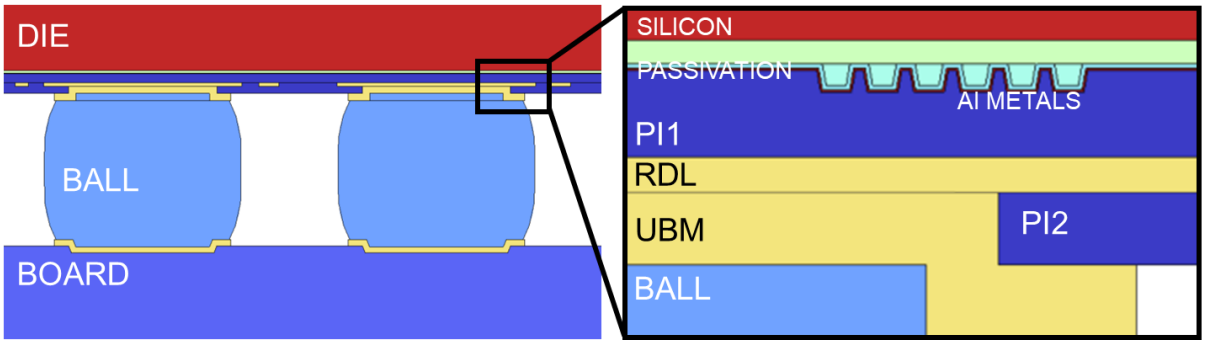

Figure 1. Cross section of a WLCSP FANIN package system; two layers of PI and one RDL is present on top of a die with Al final metallizations. UBM is present on both sides to allow ball soldering on die and on application board.

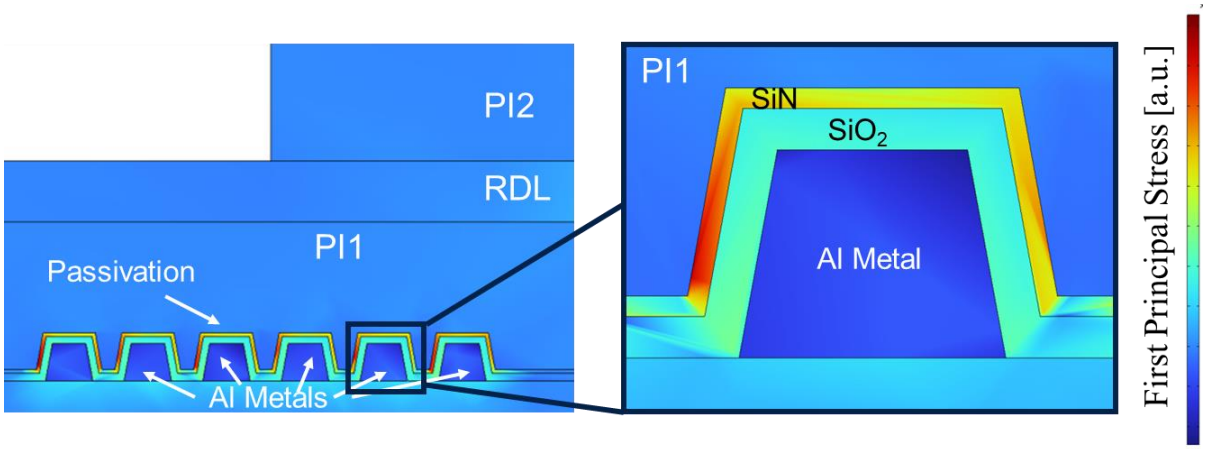

Figure 2. First Principal Stress at PI2 curing temperature; high stress found in SiN passivation layer.