Silicidation of Next Generation of FD-SOI Devices: Effect of P Doping Level in epitaxial Si:P Films

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For the next generation of Fully Depleted Silicon On Insulator (FD-SOI) and Complementary Metal Oxide Semiconductor (CMOS) devices, advanced epitaxial processes with in-situ P-doped Si layers (for nMOS) have been developed to achieve ultra-low Raised Source and Drain (RSD) access resistance [1]. To date, Ni(Pt)-based silicides have been the reference contacts for FD-SOI devices. The doping process, i.e. ion implantation vs. in-situ, is known to affect the silicidation process [2]. For in-situ doped samples, phosphorus segregation was observed at the NiPt surface, and at the NiPt/Ni_2Si and Ni_2Si/Si interfaces after RTA1, but also at the NiSi surface and at the NiSi/Si interface after DSA2. In addition, the total NiSi thickness was measured to be thinner when formed on the in-situ doped silicon [3]. In this work, we study NiPt-based silicidation on 2 generations of Si:P epitaxy.

30 nm thick Si:P films were grown by epitaxy in a 300 mm RP-CVD chamber. Two generations of epitaxy with different doping levels were investigated. Gen #A results in low doped Si:P epilayers with a phosphorus content of about 0.3%, while Gen #B is a high doped Si:P epilayer with about 4% P. After cleaning in HF 0.5% solution followed by in-situ Siconi process, metallization of these Si:P films was performed using $Ni_{0.9}Pt_{0.1}$ metal (7 nm) capped with 7 nm TiN deposited using magnetron sputtering RF-PVD chambers. The wafers were then annealed by Rapid Thermal Annealing (RTA) processes at temperatures ranging from 200 to 450 °C for 20 s under an N_2 atmosphere. Finally, the samples were treated with hot sulfuric peroxide mixture solution to remove unreacted metals. We characterized the samples using four-point probe (sheet resistance measurements, R_{sh}), X-ray reflectivity (XRR), X-ray diffraction (XRD), and time-of-flight secondary ion mass spectrometry (TOF-SIMS) analyses.

Figure 1 shows the sheet resistance as a function of annealing temperature after selective etching (SE). At low temperatures, a shift in R_{sh} values between high and low doped Si:P samples is observed. This may be due to the different P content in the SiP layers. Between 200 °C and 250 °C, we see an increase in resistance for both samples. Between 250 °C and 300 °C, low-doped samples show a drop in resistivity (from 80 to 27 ohm/sq), while high-doped samples remain stable around 65 ohm/sq. The drop for the highly doped samples is observed between 300 °C and 350 °C. This R_{sh} evolution corresponds to the transition from the Ni-rich phase to NiSi. A plateau is reached at 20 ohm/sq, at 350 °C for low-doped and 400 °C for high-doped layers. This difference in behavior may be due to different levels of phosphorus. As observed by M. Lemang et al., the phosphorus could reduce the nickel diffusion rate because nickel and phosphorus could use the same diffusion pathways. These results are consistent with previous work by [4]. To confirm the phase change from the R_{sh} measurements, in-situ XRD was performed from room temperature to 500 °C with a 5 °C step (Figure 2). It shows the presence of NiPt and TiN in the XRD diagrams from room temperature to 150 °C. By increasing the temperature, the signal of NiPt disappears and the signal of NiSi appears at 250 °C for low-doped sample. The NiSi phase appears at a higher temperature, 350 °C, for the highly doped samples. This is in good correlation with the R_{sh} results, showing that the high P content delays the formation of the monosilicide. To investigate the distribution of phosphorus and its role in the phase change delay, samples were analyzed by TOF-SIMS. The SIMS profile of the low-doped sample annealed at 350 °C is shown in Figure 3. We observed phosphorus segregation at the NiSi/Si interface. This behavior is similar to that presented in [3], reinforcing the role of P as a retarder of the NiSi phase transformation.
By combining different characterization methods, we observed discrepancies between the silicidation of the 2 generations of Si:P epitaxy. We will discuss this further during the conference.

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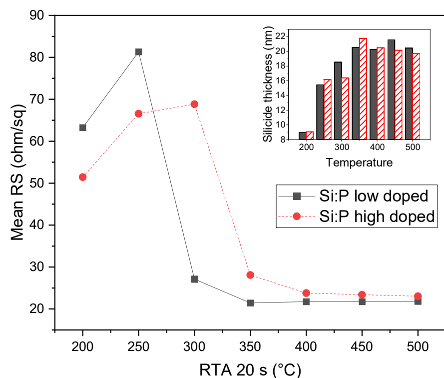

Figure 1: Sheet resistance evolution as a function of RTA temperature after selective etching.The inset shows the evolution of the silicide thickness measured by XRR with RTA temperature.

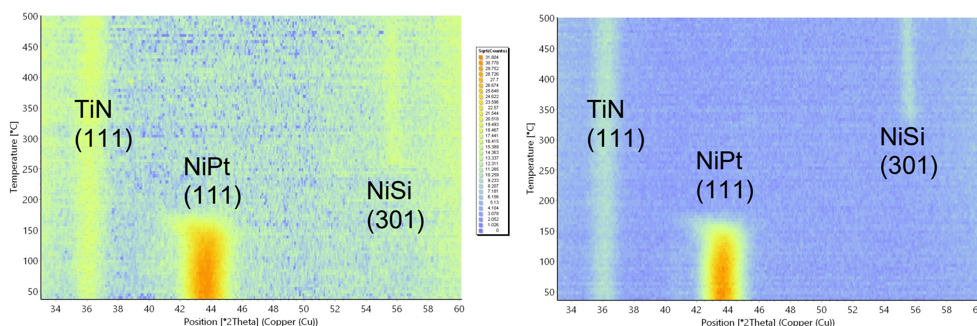

Figure 2: In-situ XRD θ-2θ diagrams during the annealing of a 7nm TiN + 7nm $Ni_{0.9}Pt_{0.1}$ film deposited on a phosphorus Si:P Gen#A (left) and Si:P Gen#B doped epitaxial layer (right).

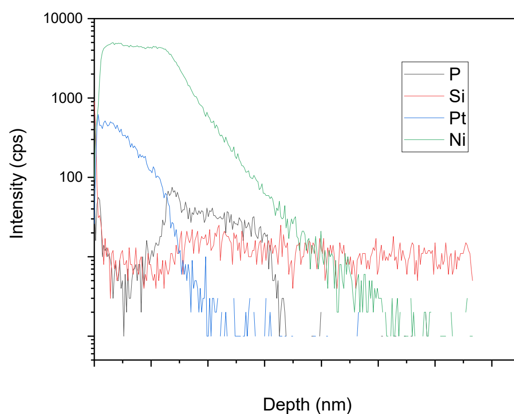

Figure 3: TOF-SIMS analysis of the NiPtSi / Si:P Gen#A stack annealed at 350°C for 20 s in N_2 and after selective etching.

References

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