Innovative approaches on TiSi-based contact development for µTrench IGBT technology: C54-$TiSi_2$ to TiSi phase transition

Davide Fagiani[a,*], Simone Dario Mariani[a], Magali Gregoire[b], Adrien Estellon[b], Marina Richet[b], Céline Borowiak[b], Mario Pistoni[a], Manuel Isacchi[a], Letterio Fiore[c], Silvia Cannizzaro[c], Paola Zuliani[a]

[a] *Power and Discretes R&D - STMicroelectronics, Via Olivetti, Agrate, 20864, Italy*
[b] *Crolles 300 mm operations - STMicroelectronics, Rue Jean Monnet, Crolles, 38920, France*
[c] *Power and Discretes R&D - STMicroelectronics, Stradale Primosole, Catania, 95121, Italy*

In the frame of power technologies development, new Isolated Gate Bipolar Transistor (IGBT) technology uses large W plugs realized through a micro trench (µTRC) approach. In IGBT devices is fundamental to short circuit the p-type implanted region, known as body, with n-type implanted region, called source (Fig. 1a and Fig. 1b). When the holes travel from the body region and create a large enough forward bias voltage at junction J1 (Fig. 1a), the parasitic n-p-n transistor could be turned on. In this case the IGBT works as a thyristor, the gate loses control on the current leading to device destruction by excessive power dissipation. To avoid this destructive phenomenon, contact resistance with body and source must be minimized.
Ti based silicide has been widely used to provide an ohmic contact to the active Si regions. Ti/TiN bilayer, usually used as diffusion barrier inside W contacts, has been employed as a reactive metal layer to form titanium silicide-based contacts [1,2]. Two well-known stable phases of Ti based silicide are C49-$TiSi_2$ and C54-$TiSi_2$. With this respect, the estimated intrinsic resistivity for TiSi phase is three times higher than the C49-$TiSi_2$ one (around 60 µΩ.cm) and twelve times higher than the C54-$TiSi_2$ phase (around 15 µΩ.cm) on blanket wafers [1].
With planar contacts where silicide formation is provided only on bottom-contact surface, specific process integration aimed to obtain C54-$TiSi_2$ phase is widely used, since it guarantees a stable low resistive phase [3]. This integration includes: contact etch patterning, pre-deposition cleaning, deposition of Ti/TiN by-layer and rapid thermal annealing (RTA) to provide Ti-Si reaction. The same integration sequence was initially used on µTRC-IGBT, which aims to realize a 3D structure with an ohmic contact both on bottom and walls of the contact. This solution generated a C54-$TiSi_2$ on µTRC bottom (Fig 2a, 2b, 2c, 2e, 2f and 3a) with low contact resistance on p-type doped silicon in body region (noted as RC_P-). However, the same solution generated high resistive interface on µTRC walls with n-type doped silicon in source region (noted RC_N+ for resistance contact on N+). Since the widely used PVD Ti is a low conformal deposition, a trial was made to increase the nominal Ti deposition thickness in order to favor a thicker Ti layer on µTRC walls. This change led to the formation of a low resistive interface with source, low RC_N+, but a dramatic increase of contact resistance measured at the bottom, i.e. high RC_P- (Fig. 4). This phenomenon is expected to be due to an excessive formation of C54-TiSi2 on the planar surface at the bottom inducing barrier cracks and depletion of p-type species during silicidation process. This might be due to the Si diffusion to Ti/Si interface and the changes induced in the junction profile.
This paper concludes that µTRC-IGBT contacts development mainly deals with a change of C54-TiSi2 to TiSi phase transition: forming TiSi phase at the µTRC bottom (Fig 2g, 2h, 2i, 2j, 2k, 2l and 3b) with a low temperature RTA, we were both able to increase the Ti deposition rate on µTRC without generating an excess of silicide on bottom (Fig 4). In fact, TiSi crystalline phase presents a lower volume with respect to TiSi2 species, avoiding contact barrier cracks and p-type junction depletion on µTRC bottom. To achieve the “3D-TiSi contacts” optimal integration, a Design of Experiment (DOE) approach was used to tackle morphological and electrical requirements, by varying the following process factors: contact pre-deposition cleaning, Ti PVD thickness, TiN thickness, RTA time and temperature. Methodology, DOE factors and robustness, silicide characterization and electrical results will be deeply discussed in the final paper.

References

[1] K. Maex, *Silicides for Integrated Circuits: TiSi2 CoSi2*, Mater. Sci. Eng. R Reports **11**, vii (1993).
[2] N. Breil et al., *Challenges of Nickel Silicidation in CMOS Technologies*, Microelectron. Eng. **137**, 79 (2015).
[3] M. Gregoire and J. Schmitt, *High Performance TiSi2 Contacts for Photodiode Integration*, (2021).

* *corresponding author e-mail: davide.fagiani@st.com*

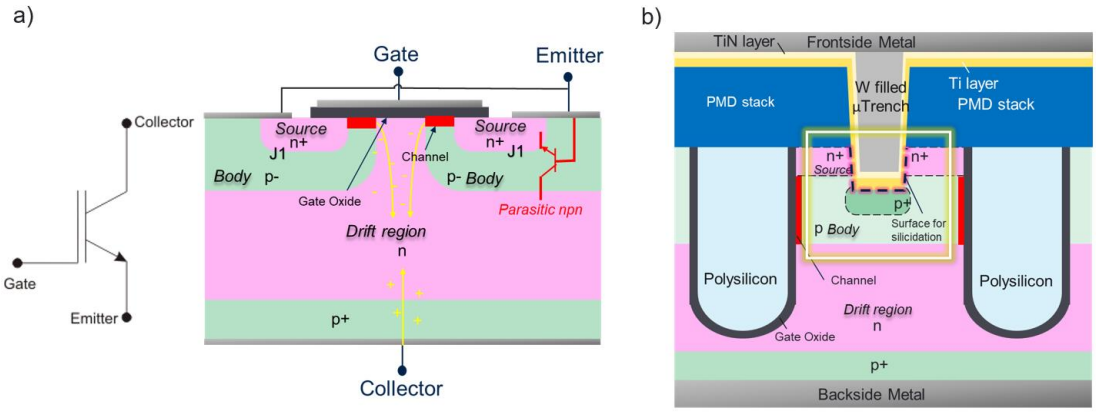

Figure 1: a) Electrical model of IGBT MOSFET presenting a wide base PNP transistor and connections between n+ and p- regions near the emitter; b)Schematic representations of W micro-trench inside IGBT devices to highlight the specific need for this technology of a "3D TiSi" formation to connect source and the body.

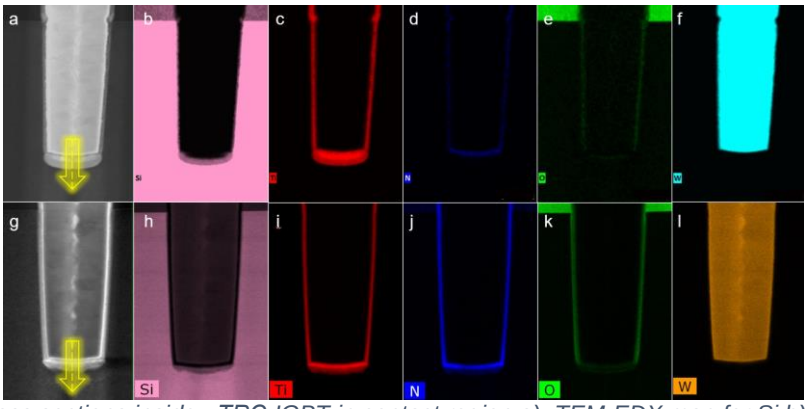

Figure 2: TEM cross sections inside µTRC-IGBT in contact region a), TEM-EDX map for Si b), Ti c), N d), O e), W f) related to $TiSi_2$ process flow; TEM cross sections inside µTRC-IGBT in contact region g), TEM-EDX map for Si h), Ti i), N j), O k), W l) related to the new TiSi process flow.

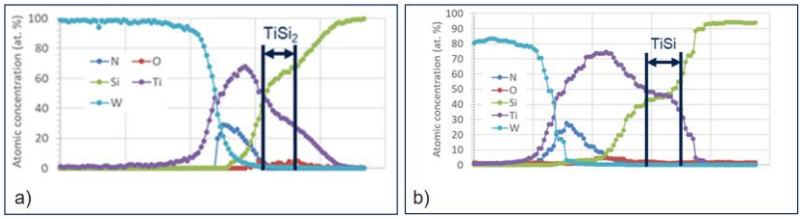

Figure 3: EDX profiles across the yellow array designed in Fig.2a a) and Fig.2g b).

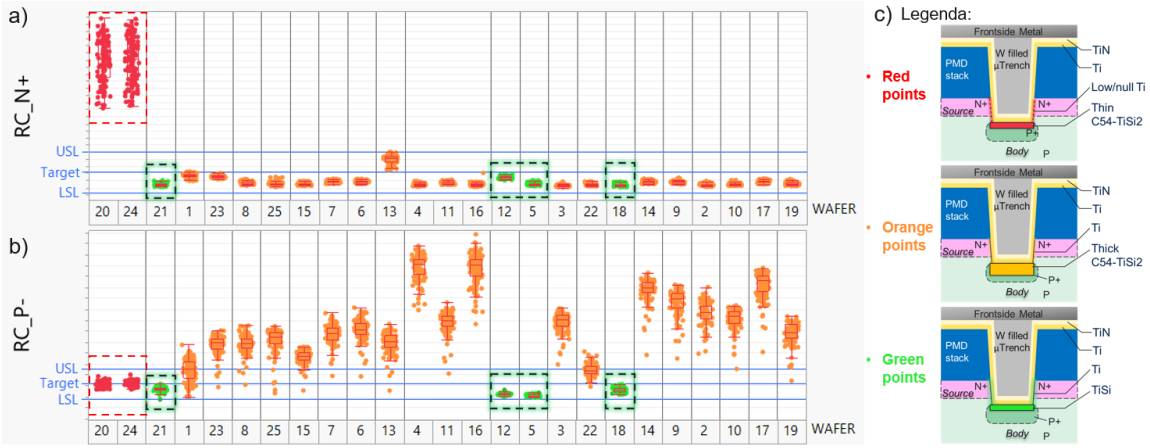

Figure 4: Contact resistance between µTRC walls and source (RC_N+) as a function of electrical DOE conditions a); contact resistance between µTRC bottom and body (RC_P-) as a function of electrical DOE conditions b); schematic representations of µTRC inside IGBT with "3D silicide" morphology as a function of electrical DOE conditions c).