Alternative Metallization: Benefits and Concerns

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What are the challenges for Cu metallization?

Cu has been the primary conductor in the logic back-end-of-line (BEOL) stack for over two decades now. For Cu, dual-damascene (DD) is the mainstream integration scheme, where a metal cladding (at the trench bottom and sidewalls) and a dielectric cap (at the top) are needed as Cu diffusion barrier and adhesion layers to ensure, among others, good dielectric and metal reliability, respectively. Scaling the thickness of these layers without compromising reliability is very challenging [1] [2] [3]. Unfortunately, metal barriers are much more resistive than Cu and dielectric caps have higher dielectric constant than the inter-metal dielectric (IMD). Consequently, line resistance, via resistance and interconnect capacitance increase with scaling [4]. The increased impact of electron scattering at interfaces and grain boundaries in narrow features (size effects) further exacerbate resistance trends. Currently, line and via resistance are widely considered to be a performance bottleneck for next-generation integrated circuits [5]. With respect to reliability, electromigration (EM) and time-dependent dielectric breakdown (TDDB) are major concerns for future technology nodes. For Cu, EM J_{Max} drops with scaling, due to smaller critical void size, larger contribution from grain boundaries (grains are smaller), and Cu wires are not expected to withstand the higher current densities required by future designs [6]. Finally, due to the leveling-off of the power supply voltage and increased impact of variability at smaller line-to-line spacing, the electric field that IMD's need to withstand at operating conditions increases with scaling and TDDB reliability margin is expected to reduce dramatically for Low-k DD [7] [8]. Although Cu will still dominate in the intermediate and upper metal levels (fat wires) for many years to come, for the lower metal levels (narrow wires) innovation in materials and processes is key for keeping pace with Moore's law and, at the same time, meeting the performance and reliability requirements which are expected with every new technology generation.

The search for the 'holy grail' metal

Alternative metals to Cu are currently being investigated for the 2nm logic technology node and beyond (metal pitch of 20nm or tighter) to mitigate the degradation of interconnect RC and reliability with dimensional scaling. Metal screening is typically based on figures of merit such as: low product of the bulk resistivity and the electron mean free path for obtaining a lower resistivity at small dimensions (lower R); high cohesive energy for enhancing EM resilience (higher J_{Max}), preventing metal drift into IMD (better TDDB) and enabling barrierless metallization (lower R) [9]; high resistance to oxidation to also get rid of dielectric caps (lower C); low intrinsic stress and good interfacial adhesion for mechanical integrity. Currently, Ru, Mo, Co and W are among the most popular candidates, as they are less disruptive options for the semiconductor industry. Their resistivity is higher than Cu at large dimensions, but size effects are less pronounced and, if barrierless, they can provide lower R than Cu at small dimensions [4]. Furthermore, barrierless via options can significantly reduce vertical resistance (lower IR-drop). Reliability prospects are also better than Cu, because of the higher cohesive energy. Process wise, different options are being considered: hybrid DD, where electroless bottom-up deposition is employed to (selectively) prefill vias with a barrierless alternative metal, followed by conventional Cu metallization; alternative DD, where Cu is fully replaced by an alternative metal in both lines and vias; Semi-Damascene (Semi-D), where direct metal etch is used to pattern a blanket film of (patternable) alternative metal, overfilling vias (to the underlying level) previously etched into an interlevel dielectric. In order to make sensible choices for future technology nodes, benefits and concerns of alternative metallization must be carefully weighed up.

Benefits and concerns of alternative metallization

Hybrid DD can provide better performance and reliability and thus extend the use of Cu metallization, which is strongly pursued by the conservative semiconductor industry. Via-prefill can indeed not only lower via resistance (due to missing bottom barrier and larger metal volume) but also facilitate Cu filling in narrow trenches (vias are already filled), which can in turn be exploited for fabricating taller lines and reducing line resistance as well. As for reliability, EM J_{Max} can be boosted, because (early) via failure modes can be avoided. On the other hand, for barrierless via-prefill metal drift into IMD is a concern for TDDB [10], [11]. Besides, in hybrid DD different metals are in contact, which raises

concerns for thermo-mechanical integrity (e.g. adhesion/delamination), stress migration and metal intermixing [12]. With respect to extendibility, Cu lines are not expected to meet EM reliability requirements at 10nm width and below [6]. Alternative DD can indeed extend reliability [13] [14] [15] [16] [17], but from a performance perspective a one-off improvement is more likely to be expected, as wire resistance would inevitably start increasing again with further dimensional scaling. This calls for more disruptive approaches. In fact, resistance trends could be potentially mitigated by targeting taller lines to compensate for a smaller line width. For DD, that is very challenging, due to trench filling limitations (voids) or dielectric pattern collapse risks (bending, zipping) [18] [19]. In contrast, for Semi-D, that is a viable option, as line aspect-ratio (AR) is controlled by the thickness of the deposited metal film and metal patterns are way stiffer. Besides, larger grains are formed, which further lower resistivity and resistance [20]. Finally, Semi-D is also a very friendly scheme for air-gaps (AG) formation (by non-conformal dielectric deposition) [21], which can be leveraged to contain capacitance increase with AR. Although RC and EM J_{Max} benefits of Ru/AG Semi-D are largely demonstrated and acknowledged by now [22] [23] [24], many concerns still remain. TDDB is no business as usual with Semi-D, because of the innovative subtractive etch process (risks of bridging/shorts) and the additional (possibly weak) interfaces that originate from self-aligned via schemes for variability mitigation [25] [26]. Another concern is joule heating: on the one hand, alternative metals can tolerate high current densities at small dimensions; on the other hand, high currents in narrow (high resistive) lines can induce high temperature [27] and high thermal gradients, which can respectively worsen EM or cause thermomigration (TM) failures in the upper (or connected) Cu metal layers [28] [29]. Self-heating is further exacerbated by the presence of air-gaps, which hinder thermal dissipation [30]. Thermo-mechanical integrity and chip-package interaction (CPI) are further concerns to be tackled [31]. Finally, sustainability aspects must be also considered, accounting not only for raw material cost but also for environmental impact (carbon emission/global warming) [32].
In this talk, we will provide an overview of in-house experimental and modeling work on alternative metallization options, covering among others performance, reliability, mechanical and thermal aspects, and discuss perspectives for future technology generations.

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