Cyclic etching processes for high selectivity and low plasma induced damage

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The challenges posed by modern patterning processes in micro-nanoelectronics are constantly increasing. In order to meet these challenges, researchers and engineers introduce new materials, evaluate original ways of integrating them and propose alternative processes. Among these, plasma etching remains essential for structuring all the wafers used to manufacture components at a nanometric scale. Used in continuous mode from its introduction in the 1970s until the end of the 2000s, pulsed or cyclic plasma etching processes are now being developed and used industrially at the most critical stages. These processes have been introduced to limit damages, to increase selectivity or to enhance the control of critical dimensions.

In this paper, we review recent developments in cyclic dry etching processes at CEA-Leti. It first briefly reminds the basic principles of plasma etching in microelectronics and then presents various strategies that have been implemented to selectively etch materials without damaging sub-layers or other materials present. These strategies involve alternating steps of adding reactants to the surface, modifying the surface or material to be etched, and removing the modified layers. The alternations can take the form of cycles or supercycles. These approaches will be illustrated by experimental results covering a wide range of applications, including the transfer of patterns formed by direct self assembly lithography [1], gate etching of III-V InGaAs transistor [2], the formation of spacers for advanced FDSOI technologies by cyclic etch [3-6] or topologic selective deposition [7,8], and the etching of contacts on quantum bit architectures on Si. Across all of these applications, the additional benefits provided by cyclic processes will be demonstrated in relation to performance indicators such as damage and/or selectivity. Furthermore, the increasing complexity of developing these approaches highlights the need for a fundamental understanding of each stage of the process. The results achieved in this area will be also discussed in term of plasma-surface interaction to better explain the etching and selectivity mechanisms.

Finally, a concluding section will present the opportunities offered by cyclic plasma etching processes to address the challenges associated with the ongoing development of FDSOI 10nm technology at CEA-Leti.

References

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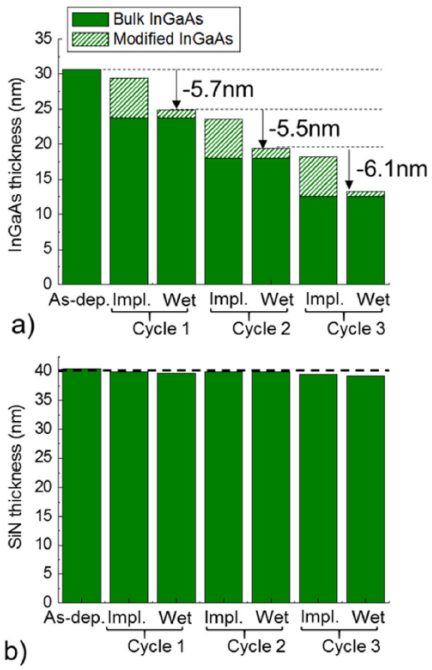

Figure 1 : Evolution of the InGaAs (a) and SiN (b) film thickness after each step composing an etch cycle, from [2]

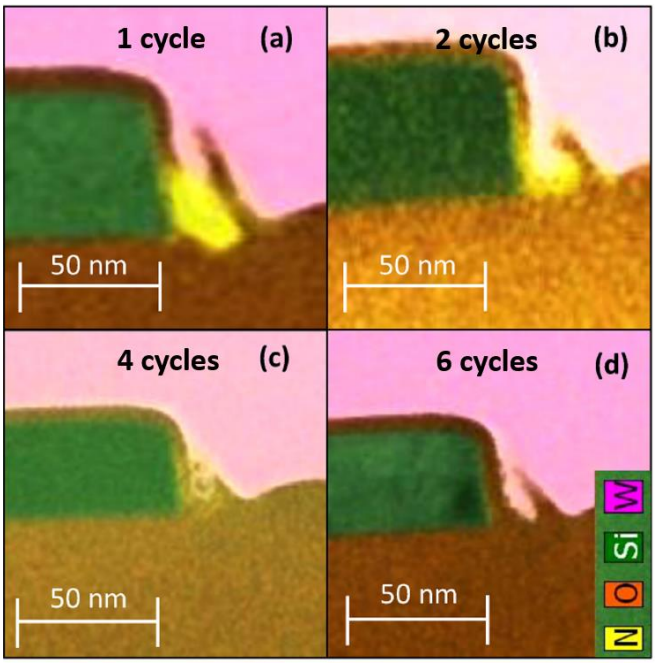

Figure 2 : TEM/EDX images showing the removal of the parasitic spacer on the side of the SOI active area after 1,2, 4 and 6 etch cycles, adapted from [6]

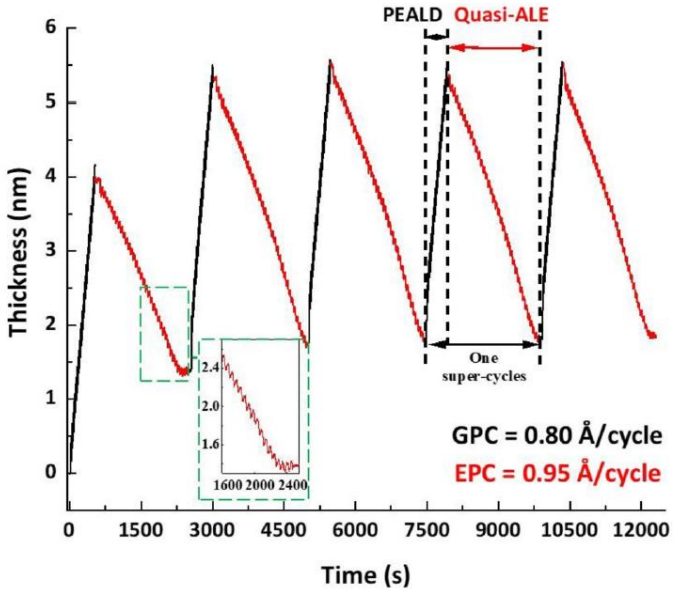

Figure 3 : In situ measurements of five Ta_2O_5 PEALD and quasi-ALE super-cycles on a planar Si substrate, from [7]