

Abhinandan Antony¹

Martin V. Gustafsson², Guilhem J. Ribeill², Matthew Ware², Anjaly Rajendran³, Luke C. G. Govia², Thomas A. Ohki², Takashi Taniguchi⁴, Kenji Watanabe⁵, James Hone¹, and Kin Chung Fong²

¹ Department of Mechanical Engineering, Columbia University, New York, NY 10027, USA

² Raytheon BBN Technologies, Quantum Engineering and Computing Group, Cambridge, Massachusetts 02138, USA

³ Department of Electrical Engineering, Columbia University, New York, NY 10027, USA

⁴ International Center for Materials Nanoarchitectonics, National Institute for Materials Science, 1-1 Namiki, Tsukuba 305-0044, Japan

⁵ Research Center for Functional Materials, National Institute for Materials Science, 1-1 Namiki, Tsukuba 305-0044, Japan

a.antony@columbia.edu

Miniaturizing transmon qubits using van der Waals materials

Quantum computers can potentially achieve an exponential speedup versus classical computers on certain computational tasks, as recently demonstrated in systems of superconducting qubits. However, these qubits have large footprints due to their large capacitor electrodes needed to suppress losses by avoiding dielectric materials. This tactic hinders scaling by increasing parasitic coupling among circuit components, degrading individual qubit addressability, and limiting the spatial density of qubits. Here, we take advantage of the unique properties of the van der Waals (vdW) materials to reduce the qubit area by a factor of > 1000 while preserving the required capacitance without increasing substantial loss. Our qubits combine conventional aluminum-based Josephson junctions with parallel-plate capacitors composed of crystalline layers of superconducting niobium diselenide (NbSe₂) and insulating hexagonal-boron nitride (hBN). We measure a vdW transmon T₁ relaxation time of 1.06 μ s, which demonstrates a path to achieve high-qubit-density quantum processors with long coherence times, and illustrates the broad utility of layered heterostructures in low-loss, high coherence quantum devices.

Figures

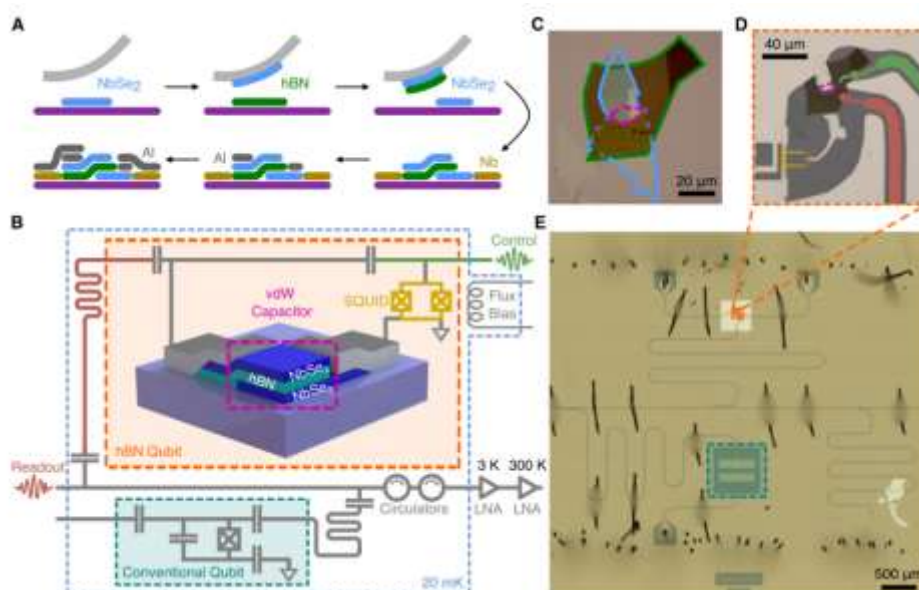


Figure 1: Fabrication of vdW transmon and measurement schematics.