

Field Control and Carrier Dynamics Near Grain Boundaries in monolayer MoS₂ Channels in Field-Effect Transistors

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Abstract

The implementation of 2D materials as channels in future nodes of the CMOS roadmap holds significant promise due to their unique electronic properties [1]. However, the formation of grain boundaries (GBs) during the growth of these 2D layers presents a substantial challenge towards single crystal growth at a wafer scale and subsequently, into their integration into CMOS devices, as GBs are known to severely impact device performance. This study provides direct experimental evidence elucidating the nature of field control near GBs in 2D materials, which is crucial for optimizing device functionality. Our work reveals localization of carrier accumulation near the segments of GBs oriented perpendicular to the channel current flow [2]. This accumulation occurs because the misoriented grain's edge forms a high energy barrier that inhibits carrier escape and simultaneously results in further increment in the barrier height. Conversely, sections of GBs parallel to the carrier flow show negligible impact on current transport, highlighting the anisotropic nature of GB effects on current transport properties. Furthermore, we investigate the behaviour of the contact potential difference (CPD) versus gate voltage (V_g) in the electron accumulation regime. At lower V_g , the interface charge is dominated by poor screening, leading to a non-monotonic CPD (V_g) behaviour. As V_g increases, improved screening effects dominate, shifting the Fermi level and resulting in a distinctive inflection point in the CPD versus V_g curve. This transition is indicative of the complex interplay between interface charge and screening effects, which are critical for understanding and optimizing carrier dynamics in 2D materials. Our findings offer valuable insights into the role of GBs in 2D channels.

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References

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