Reconfigurable Two-dimensional Floating Gate Field-effect Transistors for Highly Integrated In-memory Computing

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Logic-in-memory has been considered a promising electronic approach for efficient data processing, driving extensive research into ideal hardware architectures and their integration for high-density that can enhance computing performance. Compared with conventional electronic hardware, reconfigurable devices capable of performing multiple functions are an ideal solutions to achieve high integration beyond Moore's Law. Two-dimensional (2D) semiconductors have shown immense potential for high integration and reconfigurability due to their immunity to short-channel effects and effective electrostatic doping. In this article, we demonstrate reconfigurable and cascadable 2D floating-gate field-effect transistors (FG-FETs) for highly integrated logic-in-memory. By modulating the trapped charges within the floating gate, reconfigurable FG-FETs can achieve all types of electrical conduction, including metal, n- and p-type semiconductors, and insulators. Furthermore, a single gate terminal can execute both programming and switching operations, as well as precisely control threshold voltage shifts to enable cascading, leading to enhancing area efficiency and flexibility in circuit design. Our circuit simulations show that integrated reconfigurable computing units using cascading can operate multiple logic functions of 16 Boolean logic gates, as well as arithmetic functions as adder, subtractor, and comparator. Our work offers a potential pathway for integrating a reconfigurable logic-in-memory processor, providing an area and energy-efficient solutions for logic-in-memory computing.

Keywords: Reconfigurable and cascadable electronic device, high integration, logic-in-memory, two-dimensional semiconductor, van der Waals heterostructure