Dynamic Power Reduction in Content Addressable Memory using Differential Match-line

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Abstract

This paper proposes a differential match-line(ML) (Figure 1) and accompanying skewed sense amplifier structure for low power and high performance content addressable memory(CAM). Discharging of ML is routed to the complementary ML(MLB) for charge recycling and a differential amplifier is connected to the ML conjugates to keep the same input strength under the halved ML swing. The operating condition of the differential amplifier is aligned to maximum speed and skewed by 45mV for marginal sensing margin exploiting switching noises. A CAM with 64-bit long word lines designed in 1.8V 180nm technology proved that ML power dissipation is reduced by 45% and sensing speed is enhanced by 55% when compared to the conventional single ended ML architecture. Moreover, high speed sensing is maintained at lower VDD as low as 1.4V.

References

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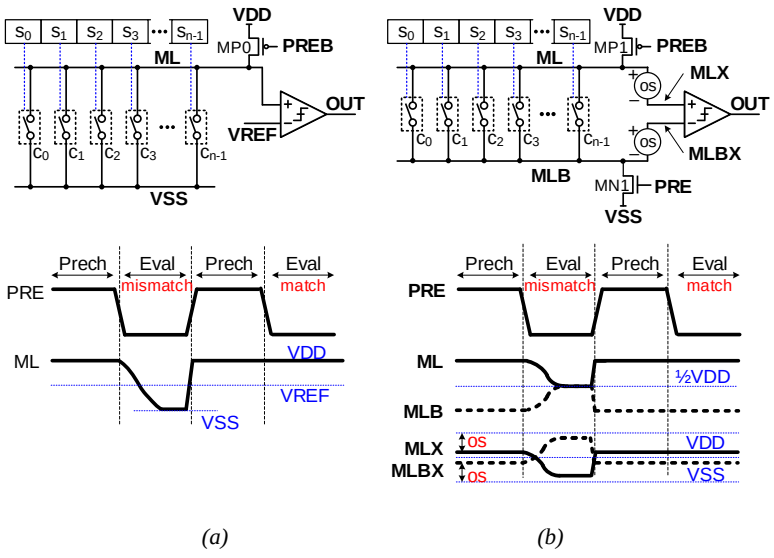
Figures



(a) *(b)*

Figure 1: Circuits and operations of NOR-type CAM with (a)single-ended and (b)proposed differential match-lines