Low temperature 2D growth and its need for the IC industry

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The increasing demand for 2D materials in the IC industry is highlighting the need for wafer-scale and fab-compatible techniques to synthesize 2D materials like graphene, h-BN and transition metal dichalcogenides. Most of recent studies indicate that high-temperature growth processes are needed to produce large 2D grains and thus better device performance [1]. The main integration scheme is nowadays the 2D growth on foreign substrates (like sapphire, metal foils, and etc) and an additional transfer step to integrate the 2D layer on a Si-compatible substrate. However, this integration scheme can cause technological limitations for some of the FAB production processes, especially if 2D would be integrated on non-planar structures (like trenches, nanowires, etc…). Furthermore, the high temperature growth of some 2D materials seems to induce more vacancy defects than low temperature processes, which, in turn, deteriorates the intrinsic properties of the material [2].

In this work, we give an overview of main CMOS applications where 2D materials are expected to play an important role. In the first part, we will describe in more details the use of 2D materials as Cu-diffusion barriers in future BEOL interconnects. Then, we highlight the barrier efficiency of our wafer-scale WS_2 grown by MOCVD. We demonstrate that crystalline 2D barrier layers can also be used as liner replacements in order to improve the metal conductivity in scaled trenches. In a second part, we will discuss the synthesis of freestanding amorphous 2D layers. We will conclude by highlighting the impact of molecular beam deposition conditions on the quality of amorphous 2D transition metal dichalcogenides.

Our results shed more light on low-temperature 2D growth and its impact on different optoelectronic applications. This is expected to play a pivotal role in pushing forward the roadmap of 2D integration into Si-CMOS technology.

References

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