

Minimum operating voltages of MoTe₂ channel/P(VDF-TrFE) ferroelectric nonvolatile memory

Yongjae Cho

Ji Hoon Park, Seongil Im

Department of Physics, Yonsei University, 50, Yonsei-ro, Seodaemun-gu, Seoul, South Korea
jae@yonsei.ac.kr

MoTe₂ channel-based P(VDF-TrFE) ferroelectric nonvolatile memory is fabricated, which operates at minimum switching pulse voltage and minimum drain voltage. For the minimum switching voltage of 8 V, bottom-gate architecture is employed and its advantages are investigated. By using bottom-gate structure, we could avoid a dead layer formed at the interface between thermally-deposited Al and P(VDF-TrFE) at top-gate architecture. A dead layer in top-gated ferroelectric memory transistors increases the coercive voltage so as the switching pulse voltage. And, for the minimum drain voltage, a novel method of H₂O₂ treatment is developed. By oxidizing the source/drain area of MoTe₂ surface by H₂O₂ solution, Ohmic contact between Pt and MoTe₂ is achieved even without thermal annealing which would have a destructive effect on the crystal quality of P(VDF-TrFE). To demonstrate the benefit of our memory transistor in aspect of power saving, it is integrated into an OLED operating circuit.

Figures

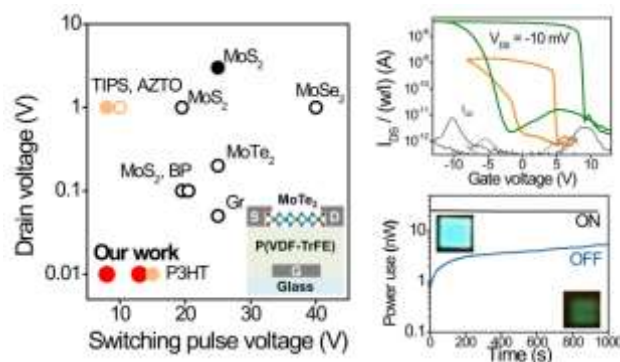


Figure 1: Comparison plot showing switching pulse and drain/operation voltages of reported non-volatile memory FETs, Memory hysteresis transfer and displacement characteristics, Power consumption-time plots of memory FETs

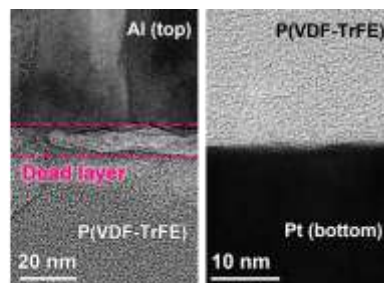


Figure 2: TEM images of P(VDF-TrFE)/metal interfaces.