

Integrating Graphene Nanoribbons on CMOS-compatible Platforms for Semiconductor Electronics

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Abstract

Graphene nanoribbons are quasi-1D strips of graphene that are tunable semiconductors and can exhibit excellent electron mobility and velocity, high current carrying capacity, thermal conductivity, and mechanical strength. Field effect transistors made of sub-10 nm wide GNRs with smooth, armchair edges can achieve higher drive current than silicon-MOSFETs and suppress short channel effects due to ultra-thin geometry. However, practical realization of commercial GNR-based technologies requires scalable, deterministic placement of GNRs on CMOS-compatible platforms. In this presentation, I will showcase some of our group's recent scientific breakthroughs towards exploiting chemical vapor deposition (CVD) – a process widely used in the industry – to achieve bottom-up synthesis of sub-10 nm wide armchair graphene nanoribbons, with smooth edges on Ge/Si(001). (1-3) By initiating the CVD growth from deterministically placed graphene nanoseeds, we have been able to precisely control the dimensions, placement and orientations of these nanoribbons and create densely aligned mesoscale assemblies of nanoribbons and nanoribbon-meshes, making it a versatile technique for large-scale production of nanoribbons for future semiconductor electronics. (4, 5)

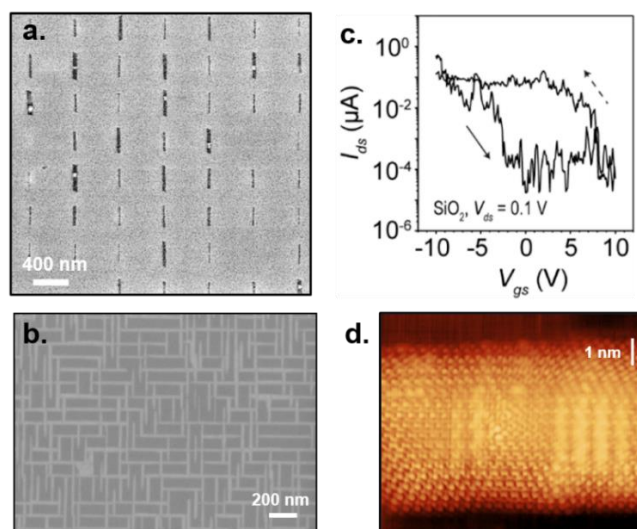


Figure 1: (a) Aligned array of CVD-synthesized graphene nanoribbons on Ge(001). (b) Bottom-up synthesized graphene nanomesh on Ge(001). (c) Transfer characteristics of a single nanoribbon FET showing an on/off conductance modulation of 2×10^4 . (d) Atomically resolved scanning tunneling topographic image of CVD-synthesized nanoribbon, showing smooth, armchair edges.

References

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