Neuromorphic and probabilistic computing with spintronic devices

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The development of more efficient and high performance spintronic devices and the efforts to have co-integration of spintronics with CMOS technology is driving the development of hybrid CMOS-spintronic solutions for applications where one can take the advantages of both technologies while minimizing their disadvantages. In this talk, I will present our recent developments on new potential applications of magnetic tunnel junctions (MTJs) in neuromorphic and probabilistic computing. For neuromorphic computing, I will discuss how to implement spiking neurons and on-chip training taking advantage of MTJ properties.
I will also focus on probabilistic computing with probabilistic-bits (p-bits) which is emerging as a computational paradigm able to be competitive in solving NP-hard combinatorial problems. I will show how to map hard combinatorial optimization problems (Max-Sat, Max-Cut, Traveling Salesman problem) into probabilistic Ising machine. We will discuss the potential of advanced annealing schemes comparing simulated annealing, parallel-tempering, and simulated-quantum-annealing and how it will be possible to implement an efficient probabilistic co-processor.

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