Resistive Memories for automotive applications

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Abstract

Emerging memories are gaining a lot of interest from academia and industry mainly by the increase of market of electronic components such as smartphones, tablets, automotive and applications such as VR, IOT, edge computing etc. With the increase of data volumes to Tbit and beyond, there is a constant research to find alternative solutions to Flash and DRAM which dominate the memory market. These technologies begin to face scaling and cost/bit limitations when applied to high volume manufacturing [1,2]. Among different alternatives proposed in the literature, Random-Access Memory (RAM) is a promising candidate. RRAM is a non-volatile memory technology, where the resistance of the memory element is modulated from conductive to insulating state by an electric field as shown in Fig. 1. In order to overcome the endurance-retention trade-off [2,3], bilayer RRAM device with resistive bilayer are proposed in literature, allowing to improve the memory performances with respect to monolayer reference technology. In reference [3,4], Al_2O_3 is studied because of the lower reset current, possibly due to a large band gap (8.9 eV) and its low power/energy consumption is attractive for memory applications. Thermal stability up to 250°C for a baking time 10^5s is shown in Fig. 2a. The high resistive state (HRS) increase is due to a longer insulating gap in the resistive layer after the RESET operation. Endurance of 10^5 cycles (compared to 10^4 cycles for the reference monolayer sample) maintaining a memory window of 1 decade is shown in Fig.2a. This improvement is due to the reduced stack degradation and the mitigated defect generation in the resistive layer during cycling [3, 4]. These properties make the technology as one of the most promising candidates among emerging memories for automotive applications. Considering the low power and cost/bit, RRAM technology is also suitable for machine learning and neuromorphic applications.

References

[1] I. Valov et al., Nanotechnology, 22 (2011), 254003
[2] G. Molas et al., IEDM 2014 Tech. Dig., pp.136-139
[3] M. Barci et al., IEEE *International Reliability Physics Symposium (*IRSP) 2014, pp. 5E-3
[4] M. Barci et al., *IEEE Journal Electron Devices Society (J-EDS) 2016*

Figures

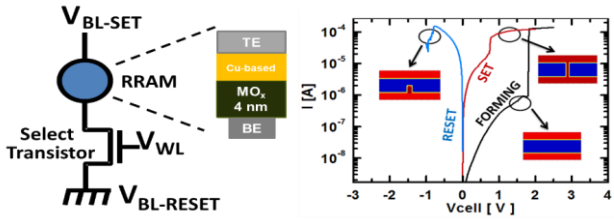
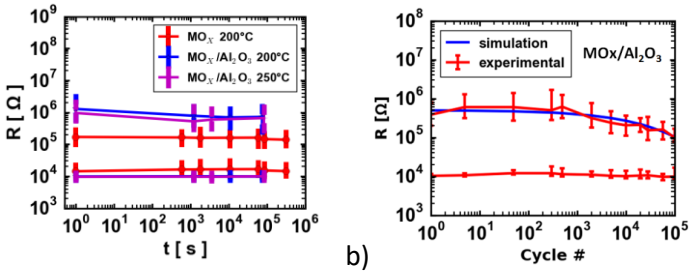


Figure 1. RRAM integrated in 1T1R configuration and its DC IV cell characteristics during SET/RESET [3].



a) b)

Figure 2. Reliability study of 1T1R array in terms of a) Endurance up to 1E5 cycles and b) Retention up to 250°C/24hrs [4].