Graphene Integration Challenges

A. Zurutuza

Graphenea Semiconductor, Paseo Mikeletegi 83, Donostia-San Sebastian, Spain

a.zurutuza@graphenea.com

Abstract

Graphene alone or in combination with other materials such as quantum dots or silicon have shown to provide enhanced performance in many applications. However, in order to integrate graphene in semiconductor devices in a cost-effective manner, it will require combining it with CMOS technology while processing the graphene into functional devices. Indeed, graphene has been monolithically integrated with CMOS technology.[1]

The fabrication of graphene at an industrial scale will require to overcome numerous challenges such as wafer scale uniformity with a high charge carrier mobility, presence of metal contamination, etc. However, wafer scale device fabrication is also critical for a successful graphene integration. At present, there is no commercial foundry able to process graphene in order to produce graphene devices (GFETs). As a consequence, we have recently launched a platform to commercialise graphene-based field effect transistor (GFETs) and thus help customers to focus on their applications rather than wasting time on graphene processing. At the same time, taking the first steps into providing a graphene commercial foundry service.

During this talk, I will cover current challenges related to wafer scale graphene growth, transfer and device fabrication.

References

[1] S. Goossens, G. Navickaite, C. Monasterio, S. Gupta, J. J. Piqueras, R. Pérez, G. Burwell, I. Nikitskiy, T. Lasanta, T. Galán1, E. Puma, A. Centeno, A. Pesquera, A. Zurutuza, G. Konstantatos and F. Koppens, Nat. Photonics 11, 366 (2017).

Figures

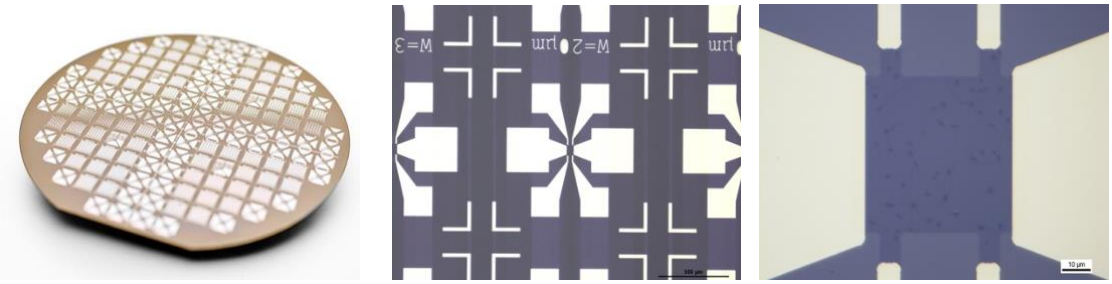

Figure 1. Wafer scale graphene field effect transistors.