Transistors and memories based on 2D materials for integrated circuits dedicated to machine learning

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In this talk we will discuss the challenges, opportunities, and the performance potential of atomistic engineering of electron devices exploiting the fundamental properties of 2D material heterostructures, with a particular attention to computer architectures for machine learning applications.

The "materials-on-demand paradigm" based on the 2D materials is a modern evolution of what in the 1980s was called "band-gap engineering" or "band-structure engineering", *i.e.*, the artificial modification of band edge profiles using heterostructures made possible by epitaxial growth of III-V and II-VI material systems.

Lateral and vertical heterostructures of 2D materials could represent a revolutionary and enabling technology to device engineering providing the possibility to engineer a transistor at the atomistic scale.

We show that field-effect transistors based on lateral heterostructures of 2D materials [1][2] and floating-gate non-volatile memories [3] based on vertical heterostructures of 2D materials for the gate stack and lateral heterostructures for the channel (as shown in Fig. 1) can represent a viable option for an integrated circuit technology dedicated to machine learning applications.

We evaluate the expected performance of the two type of devices on the basis of accepted figures of merit (Figure 2). [2][4]

The possibility of fabricating the two types of devices on the same platform and in close vicinity, can enable the fabrication of logic-in-memory architectures for deep neural networks with promising performance in terms of inferences per unit energy.

References

[1] G. Fiori et al., ACS Nano 6, 2642 (2012)
[2] D. Marian et al., Phys, Rev. Appl. 8, 54047 (2017)
[3] S. Bertolazzi et al., ACS Nano 7, 3246 (2013)
[4] G. Iannaccone et al., Nat. Nano 13, 183 (2018)

Figures

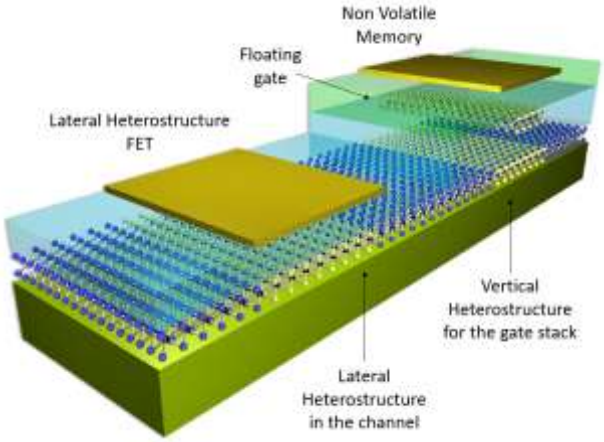

Figure 1. Illustration of the lateral heterostructure FET and of the floating-gate non-volatile memory base on lateral and vertical heterostructures of 2D materials.

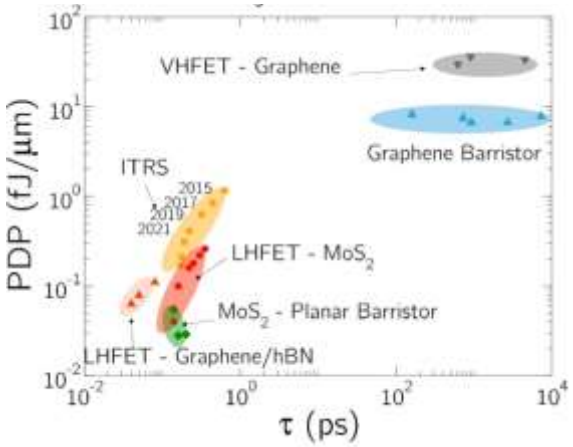

Figure 2. Power delay product (PDP) and delay time (t) of different FET structures based on heterostructures of 2D materials compared with the expectations of the International Technology Roadmap for Semiconductors (2015 edition)