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Property of MoS_2 Junction FET with $CrPS_4$ gate insulator

Abstract

As intriguing characteristics of two-dimensional (2D) materials including MoS_{2_2} and other transition metal dichalcogenides (TMDC) have been studied, the combination of 2D materials with various functional materials is attracting attention. Because 2D material is sensitive to its environment due to the nature of atomic scale material itself, controlling environments such as substrate and surface of junction with other materials is important for research and application of it. By making contact of 2D material with diverse materials, we can improve the properties of device or figure out the effects of environments. We are interested in transition metal phosphide (TMPS) which is one of the emerging materials and a new class of 2D van der Waals(vdW) materials. TMPS has a various physical properties depending on its transition metal such as magnetism and ferroelectricity. Therefore, TMPS can be considered as promising candidates to study synergistic effects when integrated with other 2D materials. Because TMPS is layered material, we can get flat and clean surface which is required for improving the properties of 2D heterostructures. In this research, we used $CrPS_4$ as a top gate insulator in MoS_2 FET device on SiO_2/Si substrate. We fabricated the FET device using e-beam lithography and evaporator and performed atomic force microscopy(AFM) to confirm the surface and thickness of MoS_2 and $CrPS_4$. In our experiment, SiO_2/Si substrate is used for back gating and Ti/Au (5 nm/ 80 nm) metals are used as gate, source, and drain electrodes of FET device. *I-V* characteristics shows the electrical properties of the device with and without junction of $CrPS_4$. The mobility with $CrPS_4$ is 6 times higher than without it for back-gated FET and on/off ratio is about 10^6 for both of them which is high enough. We also measured top-gated *I-V* curve using $CrPS_4$ as a gate insulator. Leakage current level is 10^{-11} A, on/off ratio is 2.1 x 10^5 and the subthreshold swing (SS) is 1.06 V/dec which is lower than in back-gated FET. In dual-gated FET, top gate voltage is applied with changing doping level of MoS_2 channel by back gating. Our results confirm that $CrPS_4$ can be used as gate insulator and junction material to improve the performance of FET device based on 2D material. Furthermore, we can study more interesting physical phenomena in this junction FET device by precisely controlling temperature or external field. This study will help us to find a way to improve properties of 2D materials, study about effects of its environments and possibility for its potential applications.

Figures

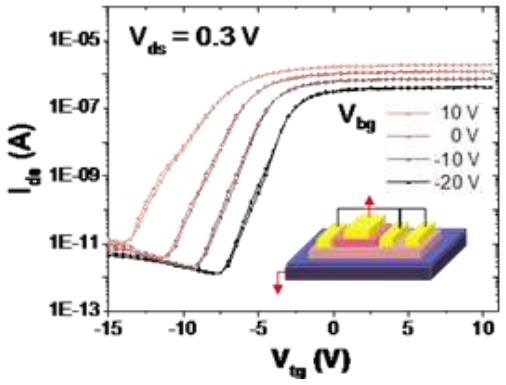

Figure 1: Dual-gated I-V curve of MoS_2 FET with $CrPS_4$