Gwang Hyuk Shin
Hamin Park, Khang June Lee, Sung-Yool Choi*
KAIST, 291, Daehak-ro, Yuseong-gu, Daejeon, Republic of Korea

sungyool.choi@kaist.ac.kr

Vertical tunneling field effect transistor based on Si-MoS_2 van der Waals heterojunction

As the technology of artificial intelligence (AI) has been developed, the efficiency of the hardware, which means the performance of the portable electronic device, as well as the software becomes important because the technology of AI needs a large amount of the arithmetic operation and processing the information. In this regard, we should design and develop the transistor with the low subthreshold swing (SS) and appropriate $I_{on/off}$ ratio. However, the conventional metal-oxide-semiconductor (CMOS) field-effect transistor has the physical limitation of the SS of 60 mV/dec. Therefore, we have to develop the novel device using not only the new concept of the operation mechanism but also the materials with outstanding physical properties.

Tunneling transistor is one of the promising candidates among the low-power consumption device with different operation mechanism compared to the conventional transistor. [1] The band-to-band tunneling from the valence band to the conduction band enable the SS to reduce lower than 60 mV/dec. Although the tunneling transistor could be an energy-efficient device, there are several challenges such as the low on-state current and $I_{on/off}$ ratio. In order to overcome these issues, we should design the structure as well as the materials with good properties. In terms of the structure, vertical tunneling field effect transistor can improve the on-state current because the band-to-band tunneling occurs at the surface in the heterojunction while the conventional tunneling transistor has the narrow tunneling area at the line edge. In terms of the materials, two-dimensional semiconductors recently have attracted much attention as the tunneling transistor due to good physical properties. [2]

Herein, we propose a vertical tunneling field effect transistor with low-power consumption using Si-MoS_2 van der Waals heterojunction. [3] The heterojunction was fabricated by transferring mechanically exfoliated MoS_2 flakes on patterned Si/SiO_2 wafer. The resulting structure of highly p-doped silicon and few-layer n-type MoS_2 forms sharp band edge profile due to van der Waals interface, which is helpful for the band-to-band tunneling. The tunneling transistor based on the silicon and MoS_2 heterojunction shows good performance with the lowest SS of 15 mV/dec and high Ion/off ratio of 10^7. Consequently, we present a tunneling field effect transistor using well-established Si fabrication technology and an emerging material of MoS_2. This device could reduce energy consumption and extend the application of AI.

References

[1] Ionescu et al, Nature,479 (2011) 329-337
[2] Sarkar et al, Nature,526 (2015) 91-95
[3] Shin et al, ACS applied materials interfaces, 10 (2018) 40212-40218

Figures

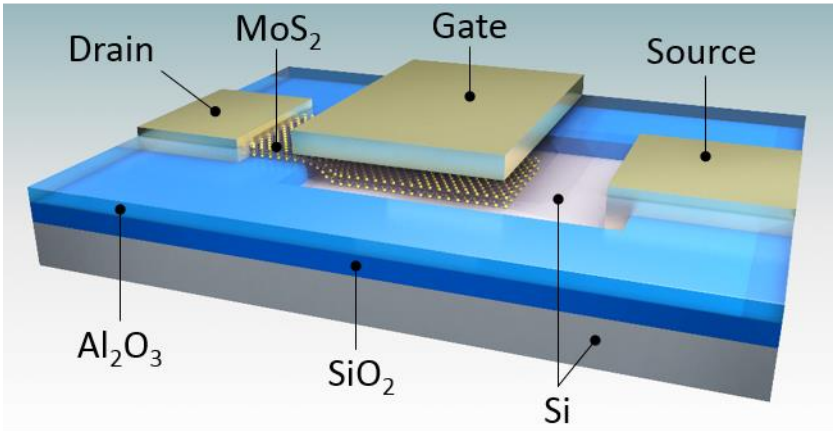

Figure 1: Schematic diagram of a vertical tunneling field effect transistor based on Si-MoS_2 van der Waals heterojunction.