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High Temperature Retention Study of MoS₂/h-BN/MoS₂ Hetero-Stack Based Non-Volatile Memory

Non-volatile memory (NVM) which can store the binary data without power supply is one of the key components in current ICT era. Since superior reliability is expected for the 2D hetero-stack based system due to its dangling bond free interface, there are some literature about 2D hetero-stack based NVM and their concepts have been demonstrated [1-4]. However, the fundamental understanding on how 2D hetero-stack based NVM is superior to the conventional 3D based NVM is quite limited. In this work, for the first step to build a thermally accelerated retention test for 2D hetero-stack based NVM, retention test was conducted over 10⁴ s at 388 K. The schematics diagrams and optical image of MoS₂/h-BN/MoS₂ based NVM are shown in **Fig. 1** and its memory operation is shown in **Fig. 2**. The inset of **Fig. 2** shows the I_d - V_{BG} curve when floating gate was grounded. Since the small hysteresis comes from the orientation polarization due to the adsorbates like water, it is clear that the large hysteresis in the main figure ($\Delta V_{th} > 30$ V) attributes to the charge trapping by MoS₂ floating gate. From the retention characteristics shown in **Fig. 3**, it is revealed that the data loss of both low resistance state (LRS) and high resistance state (HRS) is accelerated at the high temperature, and the HRS is more stable than the LRS even at 388 K. In addition, the 298 K LRS retention characteristics are not linear against time. This means the linear extrapolation could not estimate 10 years retention of 2D hetero-stack based NVM correctly. Finally, the “data loss” in previous reports are summarized against time in **Fig. 4**. The term “1st generation” refers the device structure in which 2D materials are used only as a channel, and the term “2nd generation” refers the device structure in which 2D materials are used as the channel, the tunnel insulator and FG such as shown in **Fig. 1**. From this comparison, it can be considered that 2D channel itself is not sufficient to obtain the superior non-volatility. Therefore, 2D hetero-stack structure can be better choice. Since the no significant data loss is observed even after 10⁴ s by 2D hetero-stack structure, the thermally accelerated retention test is highly required to accurate estimation of 10 years retention and discuss the degradation mechanism.

References

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- [4] Q. A. Vu *et al.*, “Two-terminal floating-gate memory with van der Waals heterostructures for ultrahigh on/off ratio”, *Nat. Commun.*, 7 (2016), 1.

Figures

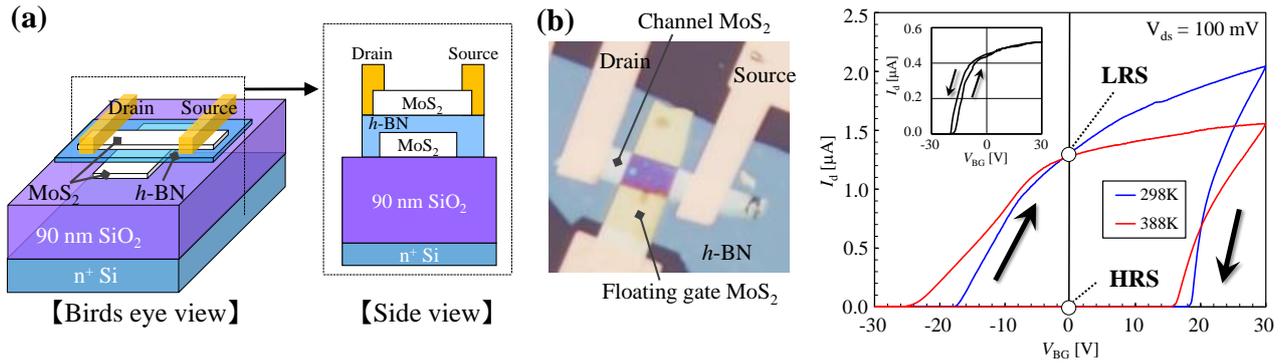


Figure 1: (a) Schematic diagram and (b) optical image of $\text{MoS}_2/\text{h-BN}/\text{MoS}_2$ hetero-stack based non-volatile memory.

Figure 2: I_d - V_{BG} curve of the NVM shown in Fig.1. The inset shows the I_d - V_{BG} curve with grounded FG at 298 K.

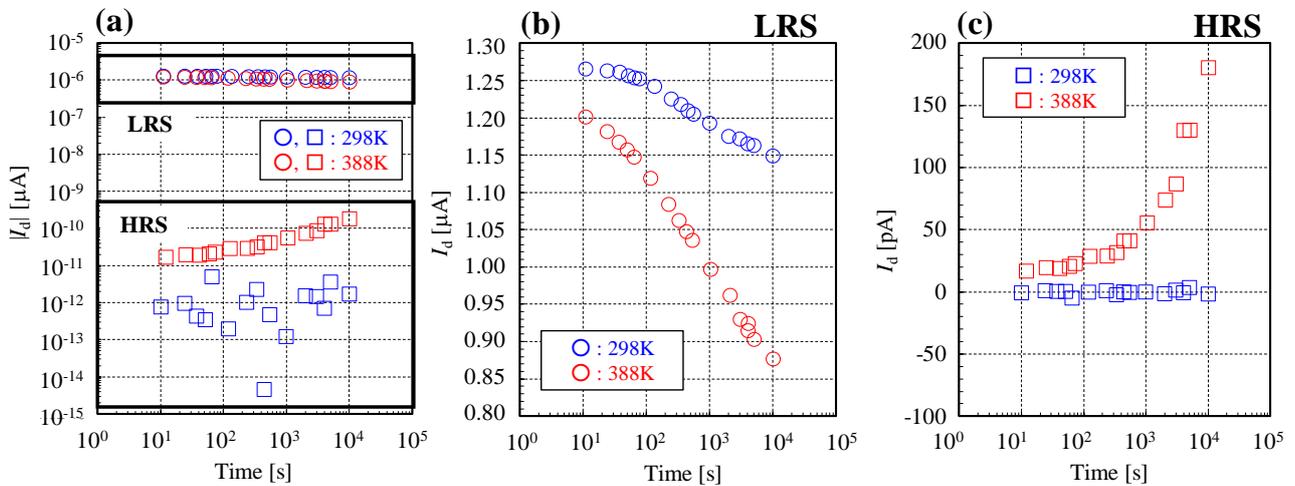


Figure 3: (a) LRS and HRS retention characteristics of 2D hetero-stack based NVM. The LRS retention characteristics are enlarged in (b) and the HRS retention characteristics are enlarged in (c).

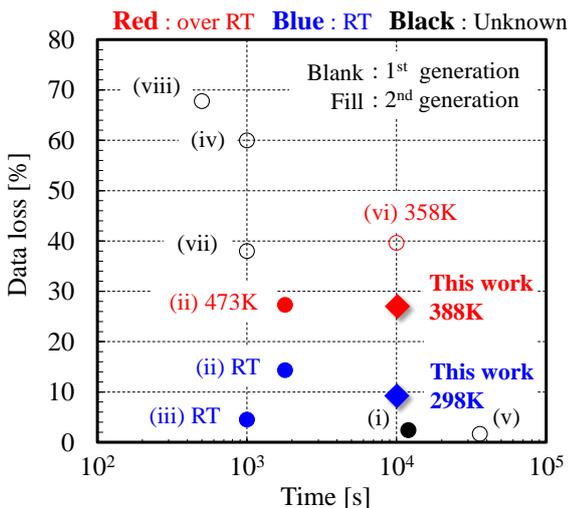


Figure 4: The data loss of charge trap based three terminals 2D-NVM devices. References are as follows.

- (format: HRS or LRS / Metrics / Literature),
- (i) LRS / I_d / *ACS Appl. Mater. Interfaces* 2018, **10**, 37, 31480.,
- (ii) LRS / I_d / *Nat. Commun.* 2013, **4**, 1624.,
- (iii) LRS / I_d / *Adv. Func. Mater.* 2015, **25**, 7360.,
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