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High-Performance InSe Transistors and its Low-Power Applications

Indium selenide (InSe) is one kind of van der Waals materials, which have garned considerable attention for developing next-generation electrions because of its high moiblity. However, its ultra-high sensitivity to surrouding media, such as O_2 or H_2O molecules, makes the existence of native oxidation on its surface, rendering to an additional charge scattering as well as a reduction of electronic performances [1]. Here, through depositing an indium (In) doping layer on the top of the InSe surface and its electrical contact area, a robust layered InSe field-effect transistor with superior controlled stability has been demonstrated. The optimized mobility can boost up to about 4000 $cm^2\ V^{-1}\ sec^{-1}$ at room temperature. Under a careful analysis of microscopic observations, the cross section of layered InSe transistors has been explored. Besides, temperature-dependent mobilitis for layered InSe transistors have been uncovered and can be explained by the dominance of the phonon scattering events, which is highly consistent with the observation of the charge noise fluctuations [2]. Evantually, the flexible functionalities with low-power operations, such as logic circuits and tribotronics [3], using the InSe transistors have been achieved. Our work reveals layered InSe materials have the potential to overcome the bottleneck in development of future electronics.

References

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Figures

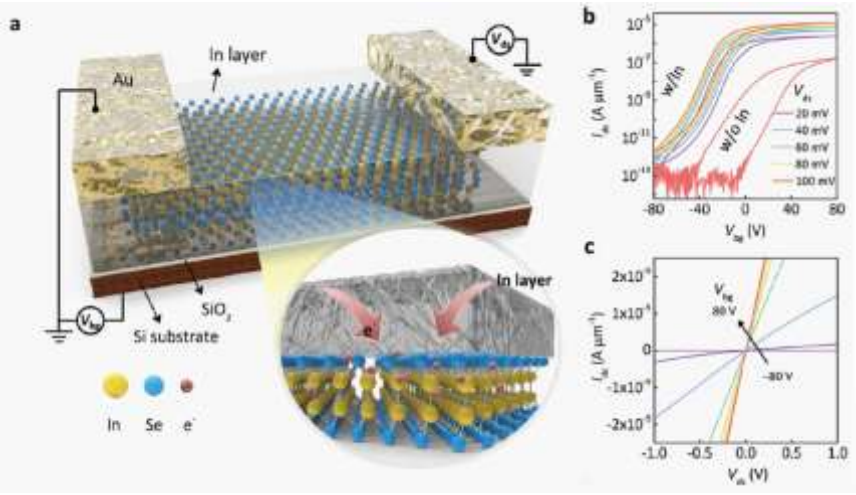

Figure 1: (a) Schematic of the InSe field-effect transistor with a deposition of In as a doping and protective layer. (b) Transfer and (c) output characterisitcs of a layered InSe transistors with 32-nm thick In layere.