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Contact Engineering of High Performance Tri-layer Indium Selenide Field Effect Transistors: Metal Deposition Induced Surface Oxide Reduction

The electrical contact has been an indispensable research topic for the development of 2D-material-based electronic devices, including field effect transistors (FETs) and photodetectors. As the dimension of devices becomes smaller, the impact of contact condition is amplified. One of the contact issues arises when evaporated metal particles cause chemical and physical interaction with underneath 2D materials, resulting in damage of these semiconducting materials and poor device performance. [1] Specifically, evaporated titanium metal particles lead to chemical reaction with underlying 2D materials during thermal evaporation process under ultrahigh vacuum condition (~10^{-9} mbar). [2] This chemical reactivity is especially critical to few-nanometer-thick layer and often leads to great degradation of the atomically thin 2D materials. To address this issue, we employ oxide interlayer between 2D semiconductor and electrode metal to study its effect on the interfacial and the transport properties of the 2D-semiconductor transistors. An oxide interlayer between 2D semiconductor and electrode metal has been shown to lower the Schottky barrier height (SBH), to achieve Fermi-level depinning, and to function as a surface passivation layer or a powerful doping agent. [3,4,5] However, it could also cause degraded transport characteristics, such as blocked carrier injection or non-Ohmic behavior in FETs. [6,7] In this work, we employ dry oxidation method to form a native oxide layer on the surface of few layer indium selenide (InSe). [4] This thin oxide layer is subsequently reacted with chemically active titanium and reduced at ultrahigh vacuum condition during metal deposition process. With this method, high-quality contact in tri-layer InSe FET is achieved, enabling high-performance transport characteristics, including Ohmic contact, low flat band SBH, and highest reported two-probe field-effect mobility of 540 $cm^2V^{-1}s^{-1}$. Consequently, we have demonstrated a novel method to combine the protective oxidation layer and reductive titanium layer to solve the metal reaction problem of titanium and to realize high performance in sub-5nm 2D semiconductors.

References

[1] Liu, Y.; Guo, J.; Zhu, E.; Liao, L.; Lee, S. J.; Ding, M.; Shakir, I.; Gambin, V.; Huang, Y.; Duan, X., Nature, 557 (2018), 696-700.

[2] McDonnell, S.; Smyth, C.; Hinkle, C. L.; Wallace, R. M., ACS Appl Mater Interfaces, 8 (2016), 8289-94.

[3] Yamamoto, M.; Nakaharai, S.; Ueno, K.; Tsukagoshi, K., Nano Lett, 16 (2016), 2720-7.

[4] Ho, P. H.; Chang, Y. R.; Chu, Y. C.; Li, M. K.; Tsai, C. A.; Wang, W. H.; Ho, C. H.; Chen, C. W.; Chiu, P. W., ACS Nano, 11 (2017), 7362-7370.

[5] Chang, Y.-R.; Ho, P.-H.; Wen, C.-Y.; Chen, T.-P.; Li, S.-S.; Wang, J.-Y.; Li, M.-K.; Tsai, C.-A.; Sankar, R.; Wang, W.-H.; Chiu, P.-W.; Chou, F.-C.; Chen, C.-W., ACS Photonics, 4 (2017), 2930-2936.

[6] Chuang, S.; Battaglia, C.; Azcatl, A.; McDonnell, S.; Kang, J. S.; Yin, X.; Tosun, M.; Kapadia, R.; Fang, H.; Wallace, R. M.; Javey, A., Nano Lett, 14 (2014), 1337-42.

[7] Ho, P.-H.; Li, M.-K.; Sankar, R.; Shih, F.-Y.; Li, S.-S.; Chang, Y.-R.; Wang, W.-H.; Chou, F.-C.; Chen, C.-W., ACS Photonics, 3 (2016), 1102-1108.

Figures

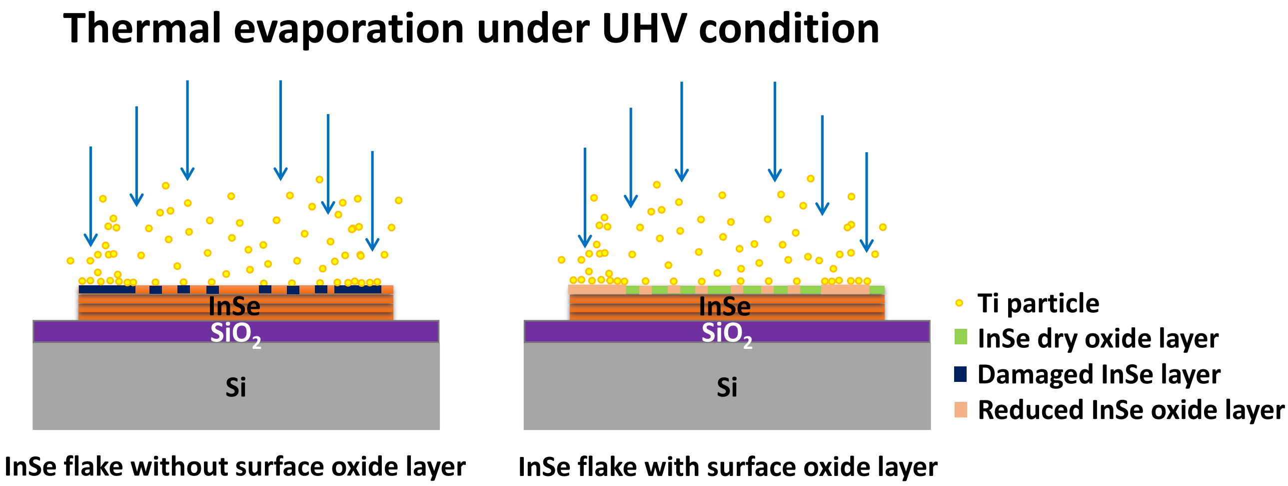

Figure 1: Schematic representation of indium selenide flakes with or without surface oxide layer. Titanium particles tend to react with InSe and damage it when there is no surface oxide layer. On the other hand, titanium particles will reduce the surface oxide layer of InSe instead if there exists an oxide layer.

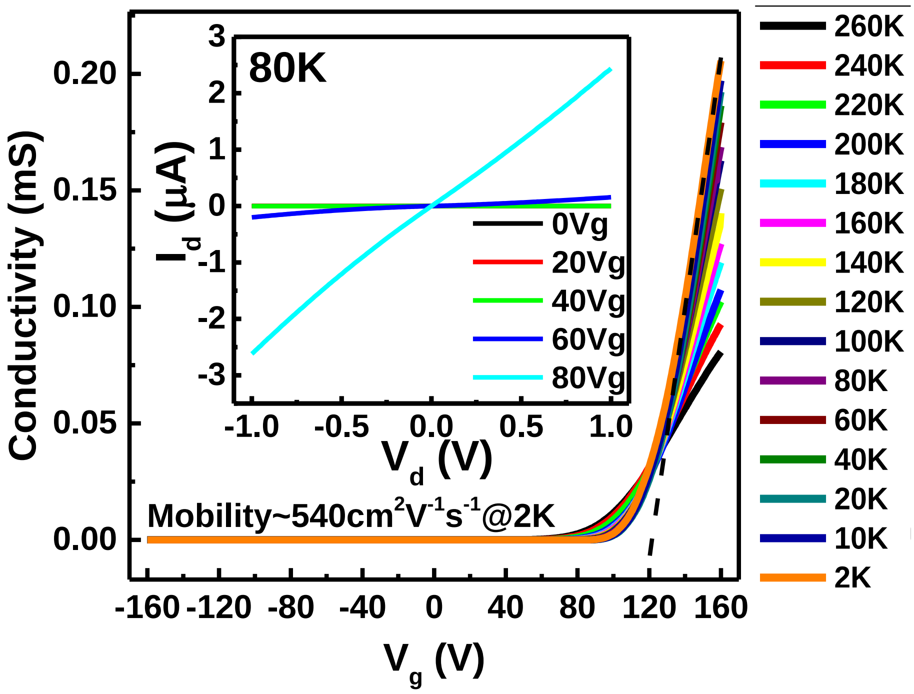

Figure 2: Evolution of conductivity versus gate-voltage curves for tri-layer InSe FET with varied temperatures. The inset plot shows the I_d-V_d curves with different gate voltages at 80K.