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Fabrication of sub-20 nm Metal Electrodes on 2D Materials without a Charged Particle Beam

Abstract
Charged particle beams for the fabrication of devices comprising sensitive nanowires or 2D materials often lead to unwanted influence or damage of electronic properties of the device [1]. Still, electron beam lithography (EBL) in combination with lift-off is the most commonly used method to fabricate prototypes of such devices.

Thermal Scanning Probe Lithography (t-SPL) [2, 3] is an alternative mask-less lithography technique which is also commercially available since 2014. It provides similar speed (up to 20 mm/s) and resolution (10 nm half-pitch) as EBL, but without charged particles involved. Here, we present two recently developed lift-off techniques for t-SPL that have enabled the creation of complex sub-20 nm Au, Pt and Ni structures and devices without the usage of high energy charged particle beams [4].

Thermal Scanning Probe Lithography (t-SPL) uses a heated silicon tip to locally decompose and evaporate a thermally responsive resist [5], usually PPA (polyphthalaldehye). A two-layer or three-layer process in combination with wet or dry etching is demonstrated to create a suitable under-cut for lift-off, respectively. During the t-SPL process the heated tip only influences the top PPA layer and leaves the underlying substrate unharmed. This is in contrast to beam based technologies like EBL or Focused Ion Beam (FIB) where most of the energy is actually deposited in the substrate and vacancies in graphene or other 2D materials can be created.
We demonstrate the capabilities of the new t-SPL lift-off processes by fabrication of transistors with improved performance (See Figure1). 50 nm wide fingered top gates have been fabricated with nanometer overlay accuracy. The superb switching behavior of the transistor shows the absence of trapped charge in the gate oxide, which usually occurs during EBL fabrication of such devices and prevents proper device operation.

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Figures

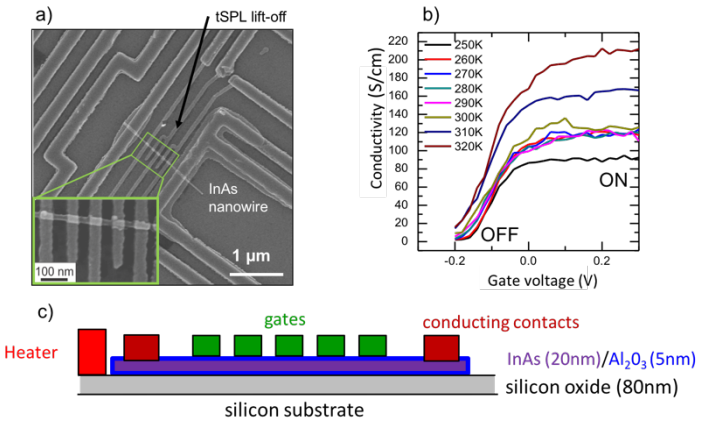

Figure 1: a) The gate electrodes of InAs nanowire transistor fabricated using the tSPL and lift-off. b) Switching behavior of the transistor. c) Schematic of the InAs nanowire transistor.