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Morphology and electrical studies on NaCl-assisted CVD synthesis of WS_2

Atomically thin two-dimensional materials such as transition metal dichalcogenides (TMDC), have been attracted a great deal of attention due to their electronic properties [1]. For the applications of various sensors and low power field effect transistors (FETs), thin films growth of TMDC with large area and uniformity is essential. Recently, alkali-metal halide assisted chemical vapor deposition (CVD) growth of TMDC have been attracted attention because alkali metal halide can reduce the density of nuclei and promote two-dimensional lateral growth [2]. In this work, I report a CVD growth of WS_2 with the assistant of NaCl and investigate the morphology and electrical characteristics of the CVD-grown WS_2.

The NaCl-assisted CVD experimental setup is shown in Fig. 1(a). WO_3 (99.99 %) precursor (~0.02 g) with one drop of 2N NaCl (~0.04 g) was put in the center of the one-zone CVD furnace. Sulfur (99.99 %) precursor (~0.5 g) was put 5 cm away from the end of the furnace and was heated with a heating tape independently. Two 285 nm SiO_2 / p^{++}-Si (100) substrates with SiO_2 surfaces facing each other were placed about ~1 cm downstream from the WO_3 precursor. One 285 nm SiO_2 / p^{++}-Si (100) substrates with SiO_2 surfaces facing down was also placed just above the WO_3 precursor. The CVD growth was performed at atmospheric pressure using 35-40 sccm 3% H_2/Ar as the carrier gas. Typical temperature programming process of WO_3 and S precursors during WS_2 growth is shown in Fig. 1(b).

The size of the CVD-grown WS_2 was estimated by optical microscope images (Fig. 2(a)). Thickness and surface morphology of the WS_2 were measured by atomic force microscope (AFM: Digital Instruments, Nanoscope IIIa) measurements (Figs. 2(b) and 2(c)). The quality of the WS_2 was evaluated by Raman spectra compared to mechanically exfoliated bulk WS_2 (Fig. 3(a)). Two different types of WS_2 deposition were observed: one was normal triangular shape WS_2 and another was WS_2 in a etched pit. The existence of the pits suggests that etching of SiO_2 occurred during the WS_2 formation process [3].

For electrical characterizations, source and drain electrodes were formed on the as-grown WS_2 by the standard photolithography process with AZ5214E photoresist (Clariant). Cr/Au (10/50 nm), Ti/Au (10/50 nm) and Au (60 nm) metal electrodes were examined. Before metal depositions, the surfaces of the WS_2 were modified by O_2 plasma treatment (5 s) performed with a resist strip system (Diener electronics, Nano). The device channel lengths were 2000-6000 nm. Figure 3(b) shows an optical microscope image of a fabricated FET with Ti/Au (10/50 nm) source and drain electrodes. Thickness and surface morphology of the WS_2 channel were estimated by AFM measurements (Figs. 3(c) and 3(d)). Electrical characterization of the WS_2 FETs was performed with a semiconductor parameter analyzer (Keithley 4200-SCS) in room temperature and under ambient conditions. Figure 4 shows drain-source (Id-Vd) characteristics at various gate voltages (Vg) for (a) pristine WS_2 FET as shown in Fig. 3, (b) the same WS_2 FET annealing at 225 °C under a 300 sccm 3% H_2/Ar gas flow for 3.5 h, (c) the same WS_2 FET additionally annealing at 225 °C under a 300 sccm 3% H_2/Ar gas flow for 2 h (Total 5.5 h). Annealing process in 3% H_2/Ar gas flow is effective for improvement of electrical contacts at metal-WS_2 interfaces. The detailed results will be discussed at the presentation.

References

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[2] S. Li, S. Wang, D. M. Tang, W. Zhao, H. Xu, L. Chu, Y. Bando, D. Golberg and G. Eda, Appl. Mater. Today, **1** (2015) 60.
[3] K. N. Kang, K. Godin and E.-H. Yang, Sci Rep., **5** (2015) 13205.

Figures

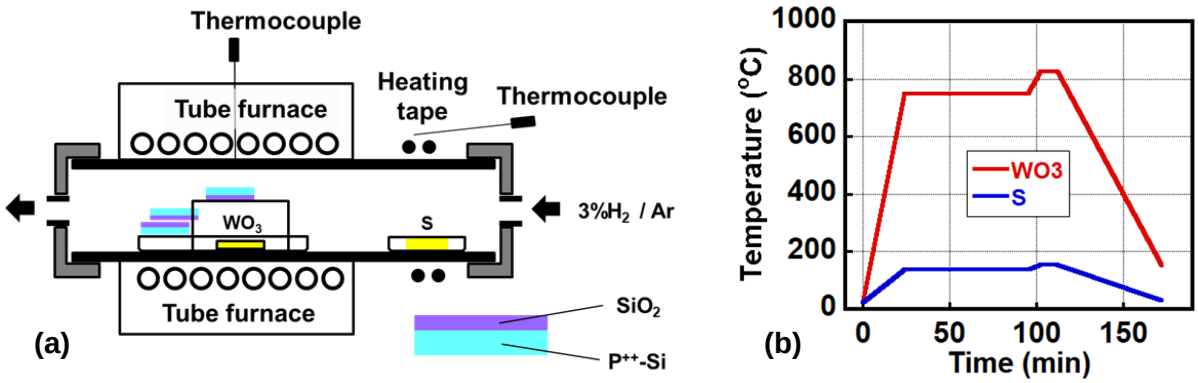

Figure 1: (a) Schematic illustration of the CVD experimental setup. (b) Temperature programming process of WO_3 and S precursors.

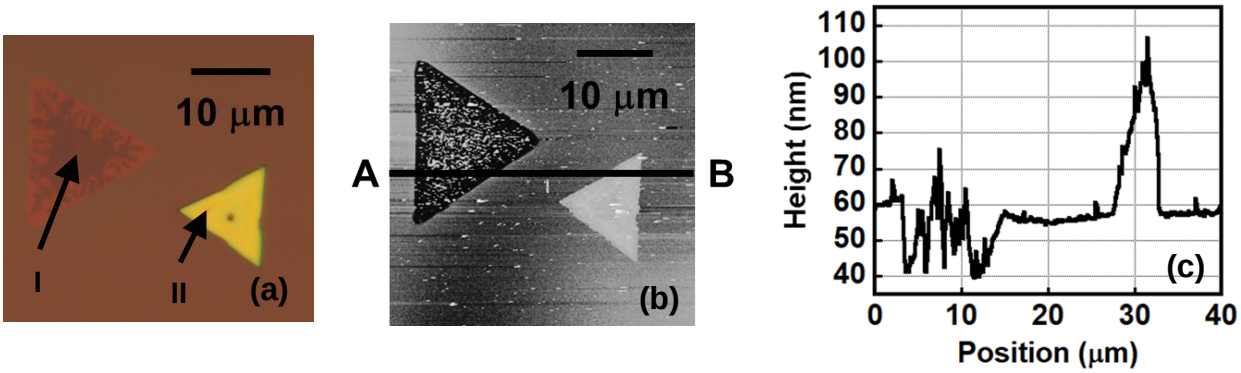

Figure 2: (a) Optical microscope image of the CVD-grown WS_2. (b) AFM image of the WS_2 at the same area in (a). (c) Cross-section profile between A and B in (b).

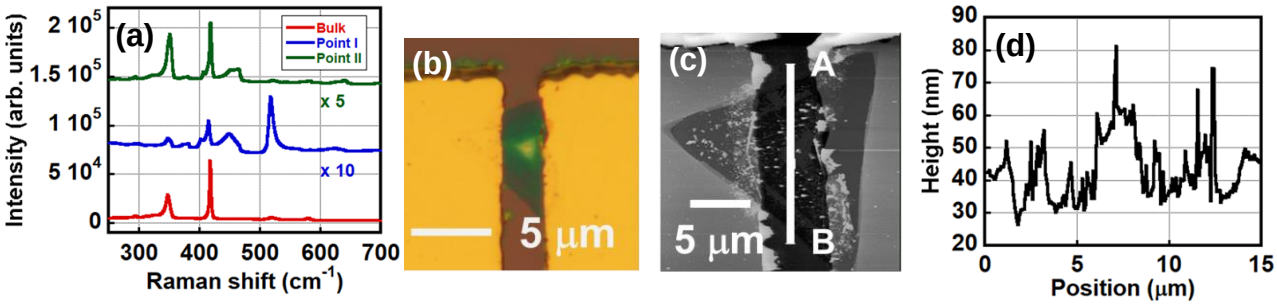

Figure 3: (a) Raman spectra of the bulk WS_2 and the CVD-grown WS_2 on SiO_2 measured at different points (I and II in Fig. 2(a)). (b) Optical microscope image of the CVD-grown WS_2 FET. (c) AFM image of the WS_2 at the same FET in (b). (d) Cross-section profile between A and B in (c).

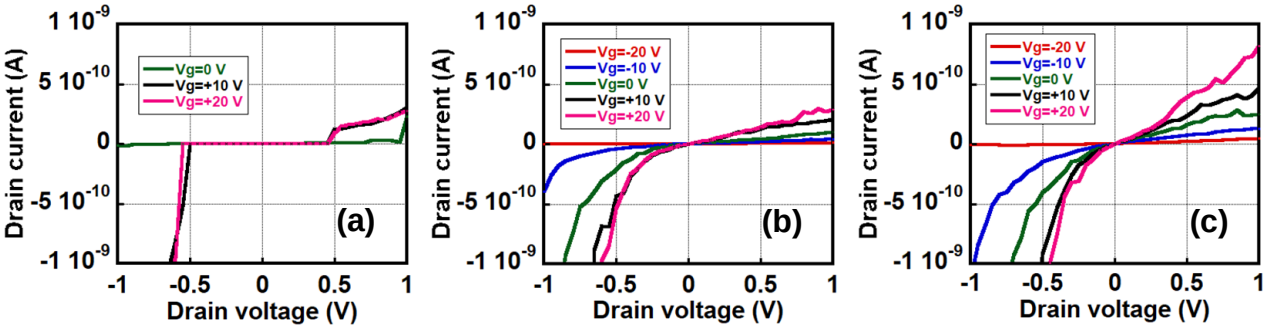

Figure 4: Drain-source (Id-Vd) characteristics at various gate voltages Vg for (a) pristine WS_2 FET as shown in Fig. 3, (b) the same WS_2 FET after annealing at 225 °C under a 300 sccm 3% H_2/Ar gas flow for 3.5 h, (c) the same WS_2 FET after additionally annealing at 225 °C under a 300 sccm 3% H_2/Ar gas flow for 2 h (Total 5.5 h).