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Promises and challenges of graphene on silicon

Graphene has a vast potential for integrated devices, promising to greatly advance the goal of ultimate system miniaturization thanks to the unique combination of its atomic thinness with its praised extraordinary functionalities such as electrical and thermal conduction, optical transparency, plasmonic response, mechanical robustness, and capacity for storing ions, just to name a few. However, the lack of a controlled and reproducible synthesis of a graphene of acceptable quality, directly on a substrate of interest such as silicon has been holding back its application for integrated systems.

Epitaxial graphene grown from silicon carbide wafers has been for long time the only route to obtain high quality graphene directly grown at the wafer –level. As far as the thermal decomposition of hetero-epitaxial SiC films on silicon wafers is concerned, this route has to-date yet to deliver an adequate graphene. We show that the use of hetero-epitaxial silicon carbide films in combination with a catalytic alloy of nickel and copper enables a consistent monolayer graphene equally on silicon with (111) and (100) surface orientations. This process can be described as a hybrid of both conventional epitaxial graphene by SiC decomposition and the growth of graphene from metal foils (schematic in Fig.1 a), specifically drawing crucial advantage from the self- limiting graphitization of the copper and liquid-phase epitaxial growth conditions [1]. This is extremely beneficial if one considers that the conventional SiC decomposition process faces critical challenges when applied to hetero-epitaxial SiC on silicon, because of the high defectivity of the SiC surface (Fig.1 b) and the fact that the decomposition temperature must be maintained safely below that of the melting point of the silicon substrate.
In contrast to the conventional growth by sublimation, this synthesis yields better graphene quality on SiC(100) and does not lead to the generation of a buffer layer on SiC(111). The catalytic alloy synthesis holds enormous promise for integrated applications, thanks to the capability for straightforward and maskless graphene patterning (Fig.2 a) [2], and to an ultrahigh adhesion of the obtained graphene to the substrate, in excess of 6 J/m^2, which is 3-fold higher than that of transferred graphene (Fig.2 b).

This approach to graphene synthesis enables the design of a broad range of miniaturised devices such as high throughput molecular recognition for bio -sensing [3], highly –performant electrodes for on-chip integrated supercapacitors [4], as well as nanophotonic devices and waveguides. On the other hand, we also point out some of the open challenges, such as the caution needed in the electrical evaluation of the graphene on SiC on silicon due to potential cross-talk issues with the substrate [5].

References

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Figures

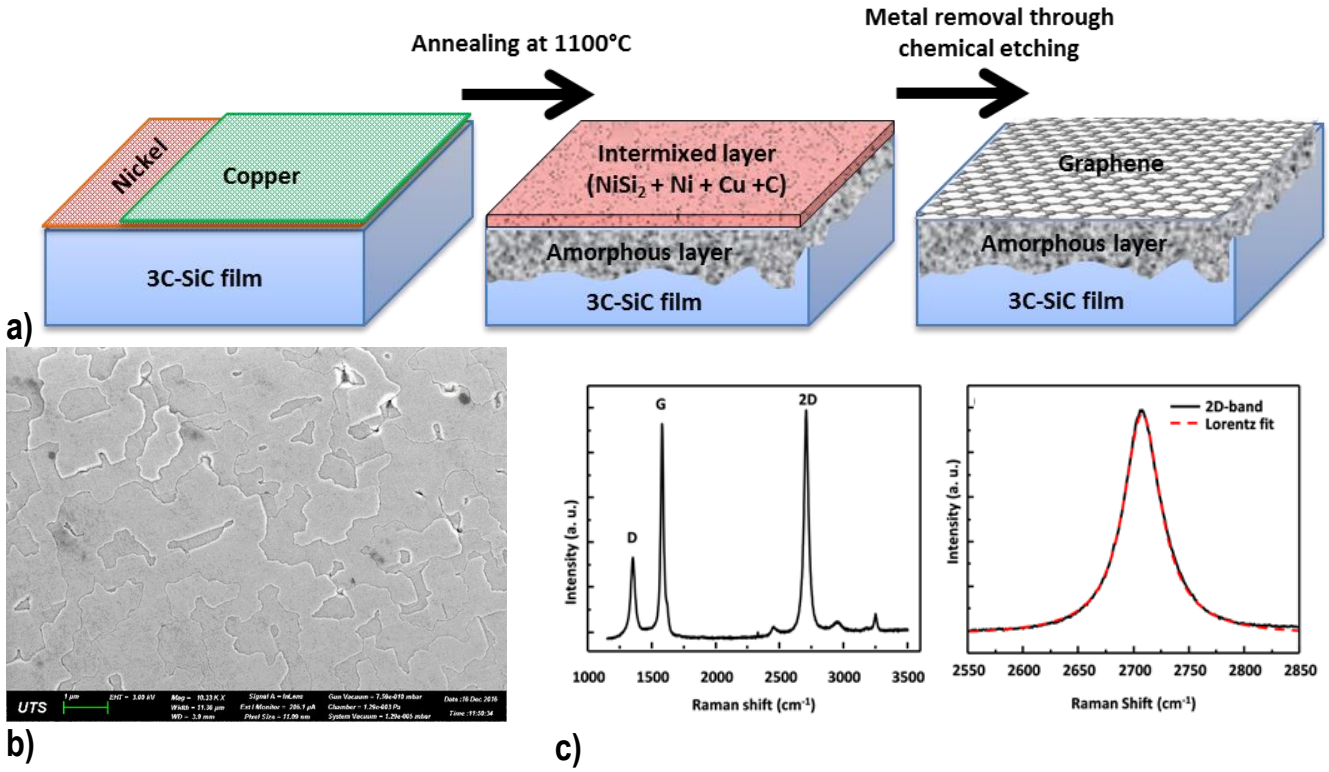
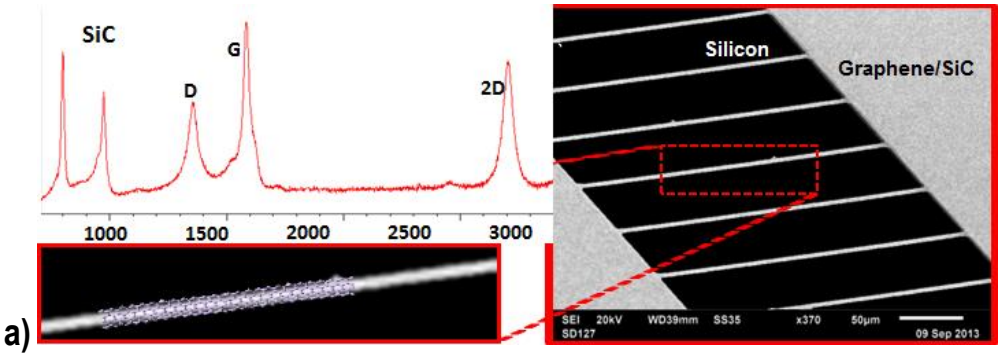


Figure 1: a) Schematic of the solid-source growth of graphene from SiC/silicon mediated a Ni/Cu alloy b) SEM top image of a SiC(100) layer, showing defects such as voids, antiphase boundaries, etc c) Raman spectra analysis of the obtained graphene, indicating a monolayer with a I_D/I_G band ratio of 0.2, as compared to the typical for graphene from thermal decomposition of SiC/silicon .



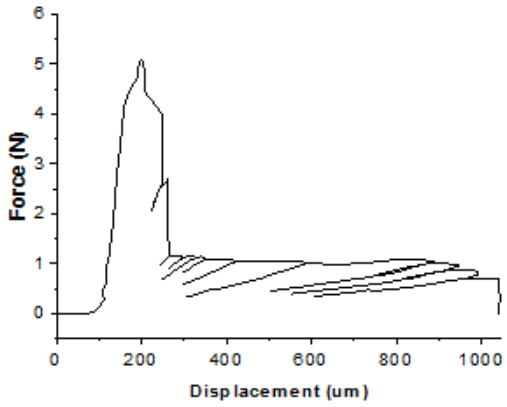


Figure 2: a) example of maskless graphene patterning through the pre-patterning of its SiC source on silicon b) double-cantilever-beam testing of graphene on SiC/silicon indicate an adhesion energy of about 6 J/m^2.