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Study of High Electric Field Breakdown Thermometry in Black Phosphorus Field Effect Transistor

The re-introduction of two-dimensional (2D) layered black phosphorus (BP) as a channel material for solid state electronic applications has excited significant interest due to its versatile properties.[1-3] BP is considered as a favorable candidate material for electronics and opto-electronic applications becasue it has thickness dependent direct band gap, strong in-plane anisotropy and high carrier mobility.[1,3] But its thermal conductivity is smaller (k~25 W/m.K) as compared to other 2D materials like graphene and MoS_2, that is good for thermoelectric applications but it causes thermal spreading problems specially at higher applied electric field.[2,5,6] Therefore, we study the heat dissipation in multilayer BP FET using highly robust electrical breakdown approach, in which the applied bias is gradually escalated to the point that physical breakdown occurs. Our measured 11 nm thick BP device (inset of Fig. a) exhibits a high current density of ~3.5×10^{10} A/m^2 that is ~ one order of magnitude higher than achieved by multilayer MoS_2. Interestingly, at high electrical field breakdown region, an unusual liner I-V curve was observed instead of current saturation as shown in Fig. a, perhaps due to new carrier generation due to impact ionization of accelerated charged carriers. By adopting a robust size dependent electro-thermal transport model, we extract interfacial thermal conductance of 1~10 M W/K.m^2 for BP-dielectic interfaces. Finally, based on our findings, we realized that most of the thermal power is deposited along the BP-SiO_2 interface while electrodes serve as efficient heat sink in operational BP FETs (Fig. b), thus an efficient thermal spreading is realized *via* dielectric engineering. Our results provide important figure-of-merits and information related to electrical breakdown and power dissipation in BP FET that are highly crucial for the design, reliability and integration of novel 2D materials for energy efficient circuits and systems.

References

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Figures

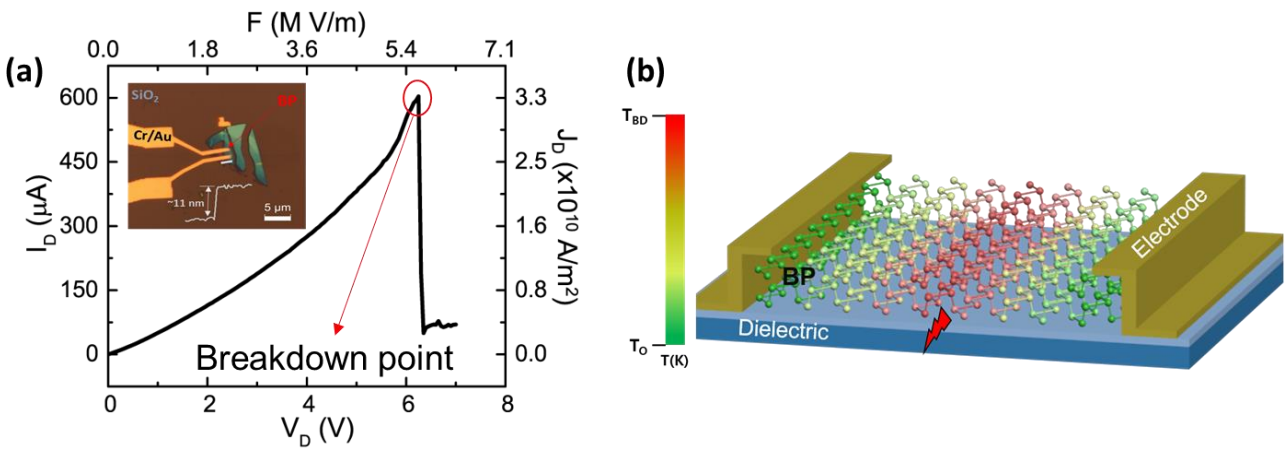

Figure 1: (a) I-V plot of multilayer back gate BP device at high applied drain bias (V_D), where red circle indicates breakdown point. **(b)** The schematic of thermal spreading in BP device.

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