Mapping of QEC – Codes in Restricted Geometries for Spin-based Quantum Technologies

Rubén M. Otxoa[1]
Arun Moncy[2,3], Reza Dasbasteh[3] and Josu Etxezarreta[3]

[1]Hitachi Cambridge Laboratory, J. J. Thomson Avenue, Cambridge, CB3 0HE, United Kingdom.
[2]Donostia International Physics Center, 20018 San Sebastian, Spain.
[3]Department of Basic Sciences, Tecnun - University of Navarra, 20018 San Sebastian, Spain.

ro274@cam.ac.uk

Abstract

Different quantum technologies have made substantial progress in the race for realizing the first Quantum Computer such as cold atoms, superconducting qubits. Qubits based on charge particles' degree of freedom has resulted as a solid contender for building a large-scale Quantum computer [1,2]. Potential scalability [3], fast operation [4] and foundries [5] with decades of experience in semiconductors physics are some of the benefits of this promising technology. However, the realization of a two-dimensional architecture layout poses several challenges in terms of wiring congestion, power dissipation and classical electronics embedding. A promising alternative lies as a short-term realization lies in architectures where the dimensionality of the system is highly restricted. Despite the fact of the inherent limitations, we propose an architecture which contains the minimum building blocks of a spin-based fault-tolerant-quantum-computer. In this contributed talk, we present an optimized mapping of some conventional quantum-error-correction codes in terms of spin-qubit shuttling [6,7] instances and avoidance of error propagation, see Figure. Moreover, we propose protocols for performing operation among embedded logical qubits under the same restricted geometry.

References

[1] D. Loss, and D. P. DiVincenzo, Phys. Rev. A **57**, 120 (1998).
[2] F. A. Zwanenburg *et al.*, Rev. Mod. Phys. **85**, 961 (2013).
[3] J. M. Boter *et al.*, Phys. Rev. Applied **18**, 024053 (2022).
[4] Weinstein, A. J. *et al.*, Nature **615**, 817–822 (2023).
[5] T. Koch *et al.*, npj Quantum Information **11**, 59 (2025).
[6] B. Jadot *et al.*, Nature Nanotechnology **16**, 570 (2021).
[7] M. Kunne *et al.*, Nat. Comm. **15**, 4977 (2024).

Figure

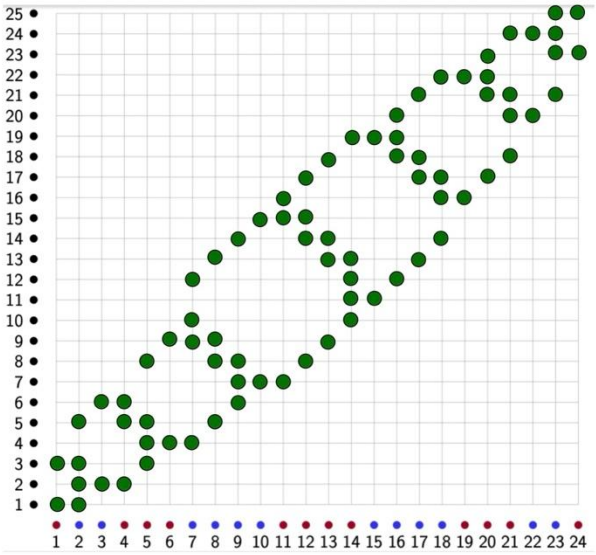

Figure 1: Map of Syndrome extraction for d=5 RSC in Train schedule, indexed as per Fig.14, showing the check qubits (blue and red) and their corresponding data qubits (black) for syndrome extraction. Each green dot is a CNOT gate.