Atomic Layer Deposition of Al_2O_3/Ta_2O_5 Multilayer Gate Dielectrics for Low-Temperature IGZO TFTs

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The implementation of a multilayer stack as the gate dielectric in a thin-film transistor (TFT) enables the resulting material to display a combination of the benefits of both materials composing the stack. With the purpose of achieving a high-κ dielectric with low leakage current and a high breakdown field, thin films consisting of Ta_2O_5 and Al_2O_3 were grown at 225 °C and 200 °C, respectively, both as multilayers and single layers, by atomic layer deposition (ALD). The rationale was to use Ta_2O_5 for a high dielectric constant, with Al_2O_3 providing a large band offset to wide bandgap oxide semiconductors as indium-gallium-zinc oxide (IGZO). The precursors/reactive elements were tantalum ethoxide, $Ta(OEt)_5$, and water for Ta_2O_5, and trimethyl-aluminium (TMA) and water for Al_2O_3. Ta_2O_5 and $Al_2O_3/Ta_2O_5/Al_2O_3$ stacked thin films were deposited in metal-insulator-metal (MIM) structures and as gate dielectrics in sputtered IGZO bottom-gate TFTs, with thickness ranging between 50 nm (single layers) and 70 nm (multilayers). The insulating thin films were characterized by capacitance and current-voltage measurements, ellipsometry and Raman spectroscopy. The ALD processes were optimized to maximize the refractive index seen by ellipsometry (denser films) and to ensure that no Raman peaks associated with residual precursor or reactant were present. The Ta_2O_5 thin films showed a dielectric constant of 20, current density of $2.66x10^{-1}$ $A.cm^{-2}$ at 1 $MV.cm^{-1}$ and breakdown field of 1.36 $MV.cm^{-1}$, the Al_2O_3 thin films showed a dielectric constant of 8, current density of $2.61x10^{-8}$ $A.cm^{-2}$ at 1 $MV.cm^{-1}$ and breakdown field higher than 4 $MV.cm^{-1}$, while the multilayer thin films exhibited a dielectric constant of 11, current density of $2.06x10^{-5}$ $A.cm^{-2}$ at 1 $MV.cm^{-1}$ and breakdown field of 2.90 $MV.cm^{-1}$. Moving to IGZO TFTs, while the Ta_2O_5 gate dielectric resulted in the largest field-effect mobility (μ_{FE}) of 20.92 $cm^2.V^{-1}.s^{-1}$, the best balance among device characteristics was achieved with the multilayer gate dielectric, which presented μ_{FE} of 12.62 $cm^2.V^{-1}.s^{-1}$, turn-on voltage (V_{on}) of 20 mV, on/off ratio>10^5, and subthreshold slope (S) of 90 $mV.dec^{-1}$. These performance metrics are similar to state-of-the-art IGZO TFTs reported worldwide, with the advantage of ultra-low operating voltage (transconductance saturation for V_{GS}<1.3 V) owing to the 70 nm thick ALD multilayer gate insulators. Regarding positive gate bias stress measurements, a negative threshold voltage shift (Δ_{VT}) during stress was verified for Ta_2O_5, similarly to our previous findings for sputtered Ta_2O_5 [1], while a positive and larger magnitude Δ_{VT} was recorded for Al_2O_3, with a lower time constant (τ). The multilayer stack revealed an interesting route to minimize stress effects, showing the lowest Δ_{VT} after 3 h stress (0.55 V) among the three gate dielectric configurations. By further tuning of the stack composition, one can achieve a complete cancelation of the two competing degradation effects of Ta_2O_5 and Al_2O_3 and suppress Δ_{VT} [2].

REFERENCES

[1] J. Martins et al., Electron. Mater. 2021, 2(1), 1-16
[2] M. Cortinhal et al., publication under preparation