

Transfer of Graphene from 200 mm Epitaxial Si/Ge(100) Wafers and it's post-processing

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Since the successful exfoliation of graphene in 2004 the research on graphene gained a lot of attention. The possibility to tune electronic properties of graphene by application of external voltage enables the engineering of Fermi level of graphene. The aim of each research topic is to find the most promising application field materials up to the industrial application level.

In this work, the main technological development and processing steps towards graphene integration in standard Si-technology processes will be presented. The main processing steps includes the graphene growth [1], its transfer by electrochemical delamination on the target wafers [2] and patterning by photolithography followed by reactive ion etching and wet cleaning processes. For the development of test structures (TLM, Hall) and test-devices (capacitors, GFETs) different contacting approaches [3] are under development in order to achieve the low contact resistance values and will be presented as well.

REFERENCES

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FIGURES

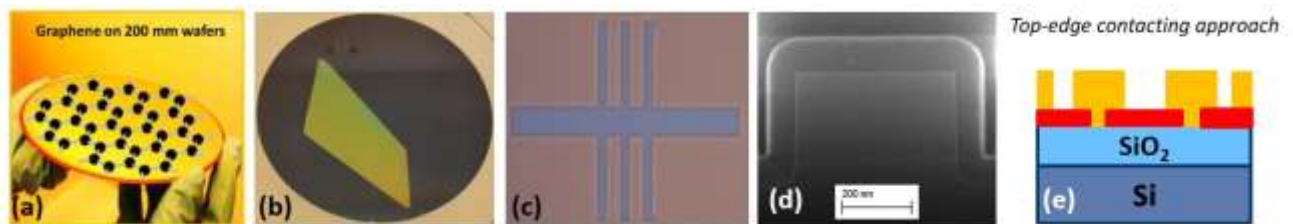


Figure 1: (a) Graphene growth on 200 mm Ge/Si wafers, (b) transferred graphene flake on 200mm SiO₂/Si wafers, (c) patterned graphene, (d) passivation of graphene with SiN, (e) graphene contacting approach through top-edge metal contacts.

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