# **Graphene Processing on Wafer Scale for Microelectronic Applications**

#### Himadri Pandey<sup>1</sup>

A. Esteki<sup>1</sup>, S. Sawallich<sup>2</sup>, B. Conran<sup>3</sup>, C. McAleese<sup>3</sup>, S. Krotkus<sup>4</sup>, S. Kataria<sup>1</sup>, M. Nagel<sup>2</sup>, M. Heuken<sup>4</sup> & M. C. Lemme<sup>1,5\*</sup>

<sup>1</sup>Chair of Electronic Devices, RWTH Aachen University, Otto-Blumenthal-Str. 2, 52074 Aachen, Germany <sup>2</sup>Protemics GmbH, Otto-Blumenthal-Str. 25, 52074 Aachen, Germany

<sup>3</sup>AIXTRON SE, Dornkaulstr. 2, 52134 Herzogenrath, Germany

<sup>4</sup>AIXTRON Ltd, Buckingway Business Park, Anderson Road, Swavesey, Cambridge CB24 4FQ, United Kingdom

<sup>5</sup>AMO GmbH, Advanced Microelectronics Center Aachen, Otto-Blumenthal-Str. 25, 52074 Aachen, Germany Email: lemme@amo.de

### Abstract

Large area chemical vapor deposited (CVD) graphene has shown immense potential for future electronic device applications [1]. However, one major problem often encountered today is the poor reproducible quality of such CVD grown layers. We report on the progress made in the GIMMIK project, where we aim to address this problem. Wafer scale graphene is grown on sapphire substrate, and quality assessment is systematically done by fabrication and characterization of electronic devices. The aim of this ongoing research project is to evolve graphene technology for electronic devices from lab to industrial levels. The weak points in the relevant processing steps are identified and ways to eliminate/minimize the sources of error are being developed. In addition, the transfer of the key graphene properties to electronic devices is continuously tested by integration into a material environment. State of the art characterization methods like tera-Hertz time domain spectroscopy (THz-TDS) are also being employed to ensure a consistent high quality graphene. Till date, Graphene sheets grown on 4" Sapphire wafers with average carrier mobility of 1700 cm<sup>2</sup>/Vs have been demonstrated. By employing CMOS compatible Nickel edge contacts to graphene [2], contact resistance values as low as 500  $\Omega$ .µm and decent sheet resistance values in the range of 800 – 1350  $\Omega/\Box$  have been observed. Lessons learnt in these steps will then be implemented on 200 mm Industrial quality wafers in future.

Support from BMBF (GIMMIK, 03XP0210) is gratefully acknowledged.

### REFERENCES

- [1] S. Kataria, S. Wagner, J. Ruhkopf, A. Gahoi, H. Pandey, R. Bornemann, S. Vaziri, A. D. Smith, M. Ostling and M. C. Lemme, Physica Status Solidi a, vol. 211, no. 11, pp. 2439–2449, 2014.
- [2] H Pandey, M Shaygan, S Sawallich, S Kataria, Z Wang, A. Noculak, M. Otto, M. Nagel, R. Negra, D. Neumaier and M. C. Lemme, IEEE Transactions on Electron Devices, vol. 65, no. 10, pp. 4129–4134, 2018.



### **FIGURES**

**Figure 1:** (a) THz-TDS assessment shows wafer scale uniform growth of Graphene on Sapphire with decent sheet resistance. (b) A typical test device used in this work. (c) These Graphene devices demonstrated average Hall mobility of 1700 cm<sup>2</sup>/Vs. Graphene used in this project was grown on 2" and 4" Sapphire wafers till date.

## GRAPHENE AND 2DM INDUSTRIAL FORUM (GIF2020)