Anatomy of 2D materials based memristors: the role of each type of defect

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Abstract
In the race of fabricating solid-state nano/micro-electronic devices using two-dimensional (2D) layered materials (LMs), achieving high yield and low device-to-device variability are the two main challenges [1-4]. Electronic devices that drive currents in-plane along the 2D-LMs (i.e. transistors, memtransistors) are strongly affected by local defects (i.e. grain boundaries, wrinkles, thickness fluctuations, polymer residues), as they create inhomogeneities and increase the device-to-device variability, resulting in a poor performance at the circuit level [5-6]. Here we show that memristors are insensitive to most types of defects in 2D-LMs, even when fabricated in academic laboratories that do not meet industrial standards. The reason is that the currents produced in these devices, which flow out-of-plane across the 2D-LM, are always driven locally by the most conductive locations. Consequently, we conclude that it is much easier to fabricate 2D-LMs based solid-state nano/micro-electronic circuits using memristors than transistors or memtransistors, not only due to the inherent simpler fabrication process (i.e. less lithography steps), but also because the local defects do not degrade the yield and variability of memristors considerably.

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