

Optical Tuning of Hole and Electron Transport in Ambipolar WSe₂ Interfaced with a Bicomponent Photochromic Layer: From High-Mobility Transistors to Flexible Multilevel Memories

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Abstract

The interfacing of two-dimensional materials (2DMs) with photochromic molecules provides an efficient solution to reversibly modulate their outstanding electronic properties and offers a versatile platform for the development of multifunctional field-effect transistors (FETs). Our work mainly focuses on 2DM-based optically switchable multilevel high-mobility FETs obtained by interfacing such 2DM with photochromic diarylethene (DAE) molecules acting as light-sensitive components (Figure 1). The efficient and reversible photochemical isomerization of the DAEs between the open and the closed isomer, featuring different energy levels, makes it possible to generate photoswitchable charge trapping levels, resulting in the tuning of charge transport through the 2DMs by alternating illumination with UV and visible light. We have demonstrate the feasibility and general applicability of our approach to optically control the transport of electrons (n-type dominant WSe₂), or holes (p-type dominant black phosphorus),^[1] or both charge carriers (ambipolar WSe₂),^[2] depending on the nature of the target 2DM. Noteworthy, the high output current modulation efficiency in ambipolar WSe₂ (97% for holes and 52% for electrons) ensures 128 distinct current levels, corresponding to a data storage capacity of 7 bit. The device is also implemented on a flexible and transparent polyethylene terephthalate substrate, rendering the 2DMs/DAEs hybrid structures promising candidates for flexible multilevel nonvolatile memories.^[2]

REFERENCES

- [1] H. Qiu, Y. Zhao, Z. Liu, M. Herder, S. Hecht, P. Samorì, *Adv. Mater.*, 31.39 (2019):1903402.
[2] H. Qiu, Z. Liu, Y. Yao, M. Herder, S. Hecht, P. Samorì, *Adv. Mater.*, 32.11 (2020):1907903.

FIGURES

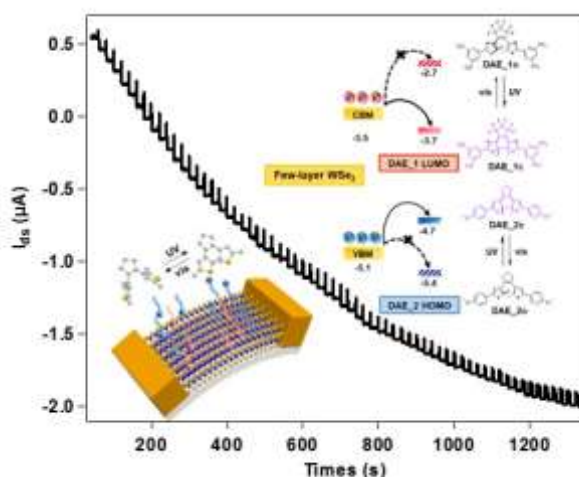


Figure 1: Dynamic output current-time curve under periodic UV irradiation. Insert is the schematic illustration of the FET device architecture based on WSe₂/DAE blend with the energy level diagram.