Setting up the ecosystem for 2D materials integration with Silicon technology

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The continual scaling of Si-based transistors has revolutionized the world through continuous breakthroughs in electronics. The Si scaling roadmap is challenged by short channel effects that limit further gate length scaling. Field-effect transistors (FETs) with semiconducting transition metal dichalcogenides (MX2, such as WS2 or MoS2) as the semiconductor channel promise however to be relatively immune to these short channel effects. FETs with 2D semiconductor channel owe this promise to the ability to make atomically thin channels combined with the theoretical ability to maintain higher carrier mobility – independent of channel thickness. These two properties give the gate voltage a better electrostatic control over the channel.
Besides this prospect of continuation of the scaling roadmap, Graphene and related 2D materials offer a heterogeneous platform for enhanced non-computational functionality monolithically integrated with silicon technology [1].

Several years ago, imec started pathfinding work on 300mm integration of both graphene modulators and MS_2-FET devices – a key requirement for industrial adoption. This work has resulted in unique 300mm test vehicles for 2D-FETs, allowing the fabrication of functioning devices with gate lengths down to 18nm [2].
These flows are used to study the impact of various processing conditions, such as the channel deposition and transfer process as well as other remaining challenges, including 2D growth quality, formation of the gate dielectric, doping and contact resistance.

This talk will give an overview on how we work out solutions in the lab which can be upscaled in the fab towards a 300mm compatible 2D technology which is compatible with the semiconductor standards.

REFERENCES

[1] “Graphene and two-dimensional materials for silicon technology” Deji Akinwande et al., Nature, sept 2019.
[2] ‘Wafer-scale integration of double gated WS2-transistors in 300mm Si CMOS fab’, I. Asselberghs et al. IEDM 2020

FIGURES

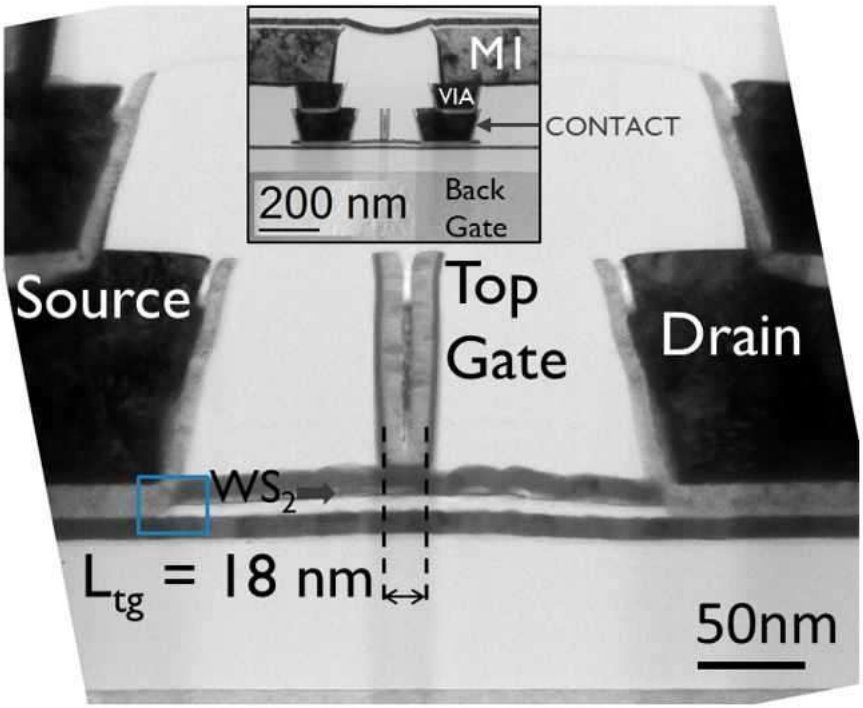

Figure 1: TEM image of 2D device fabricated with 300mm processes (imec web site).