Au cœur de l'efficacité énergétique

ElectroMagnetic Compatibility in Power Electronics: from packaging to EMC filter optimization

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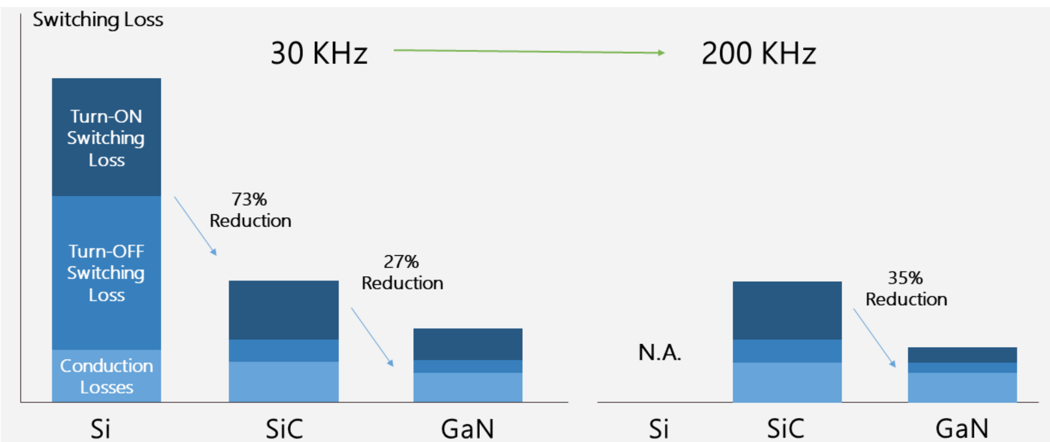
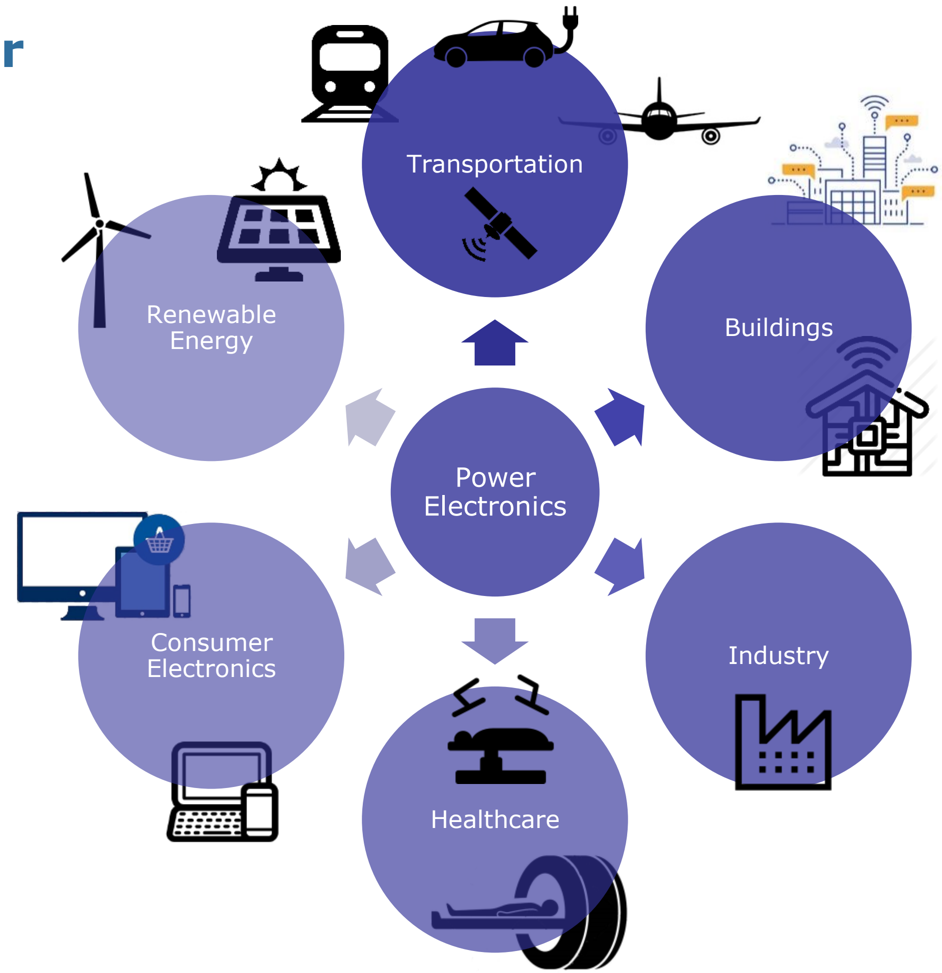
Clustering and Global Challenges (CGC2021)

Introduction

- **40% of electricity processed by power electronics**
- **Expected doubling over the next decade, reaching up to 80% by 2030**
- **Impact of Wide Bandgap revolution**

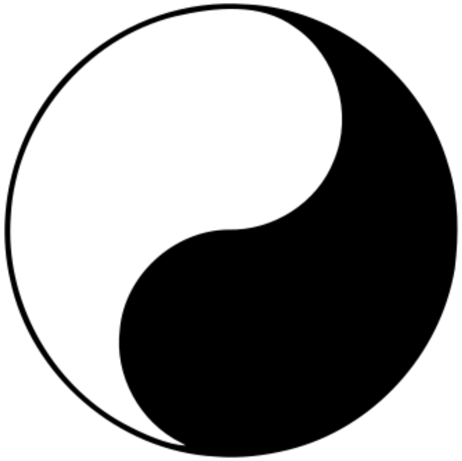


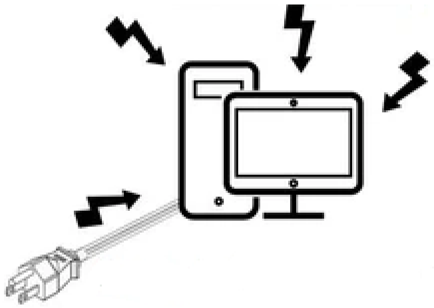
Spec Consortium, Singapore



Switched Mode Power Supply

- **High efficiency**
- **Low volume, weight**
- **High dynamic**





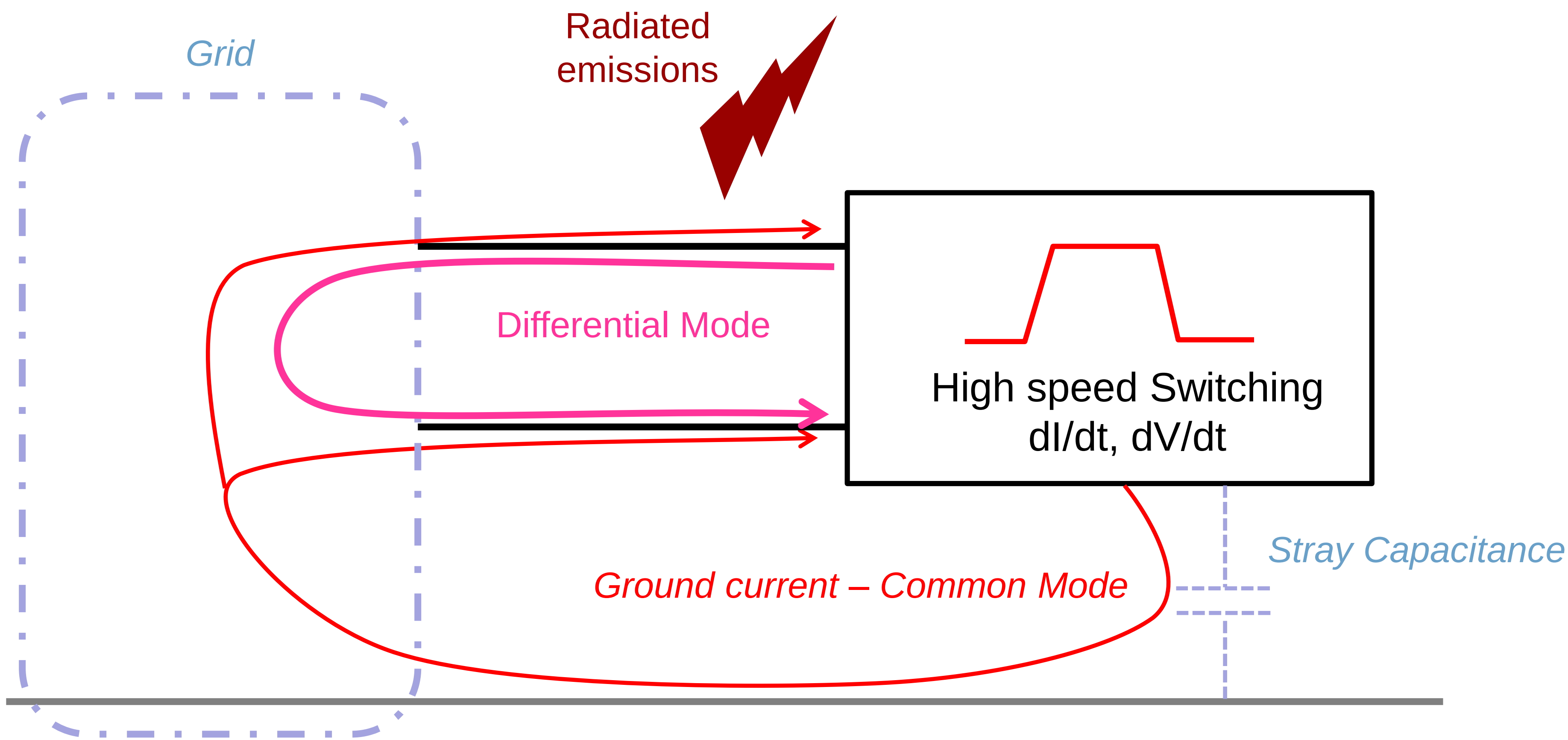
- **Electromagnetic Interferences**

Outline

1. **EMI generation principle**
2. **EMC & Semiconductor Packaging**
3. **EMC Filter design and optimization**
4. **EMC models at system level**

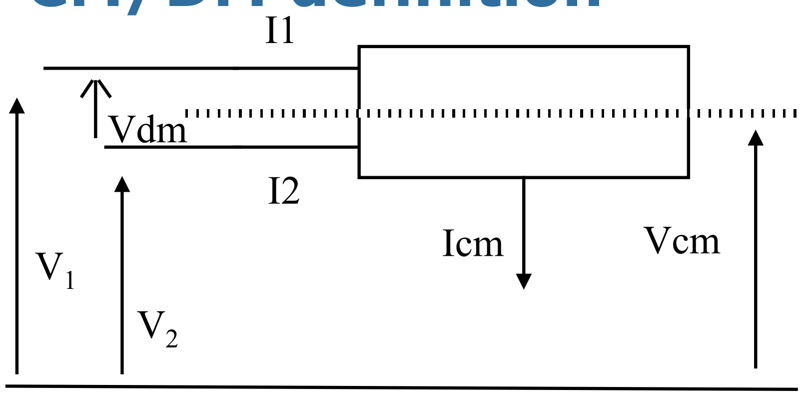
EMC: ElectroMagnetic Compatibility
EMI: ElectroMagnetic Interferences

1. EMI Generation Principle



1. EMI Generation Principle

CM/DM definition



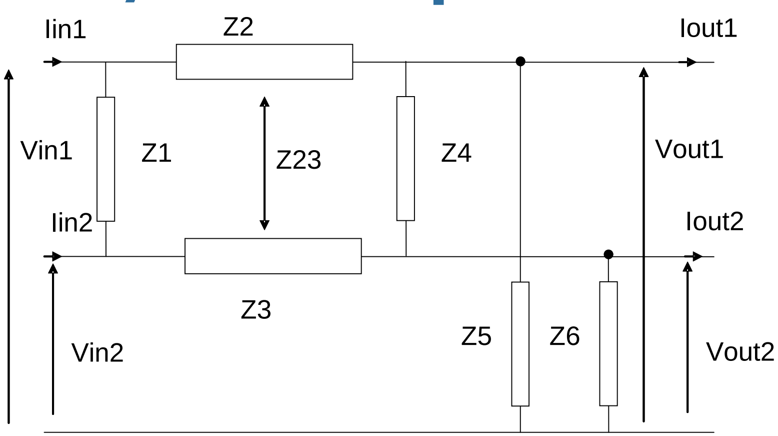
$$V_{dm} = V_1 - V_2 \qquad V_{cm} = \frac{V_1 + V_2}{2}$$

$$I_{dm} = \frac{I_1 - I_2}{2} \qquad I_{cm} = I_1 + I_2$$

$$\begin{bmatrix} V_{md} \\ I_{md} \\ V_{mc} \\ I_{mc} \end{bmatrix}_{in/out} = [P] \cdot \begin{bmatrix} V_1 \\ V_2 \\ I_1 \\ I_2 \end{bmatrix}_{in/out}$$

$$[P] = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & \frac{1}{2} & \frac{-1}{2} \\ \frac{1}{2} & \frac{1}{2} & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix}$$

CM/DM independence if symmetry



$$\begin{bmatrix} V_1 \\ V_2 \\ I_1 \\ I_2 \end{bmatrix}_{out} = [Mat] \cdot \begin{bmatrix} V_1 \\ V_2 \\ I_1 \\ I_2 \end{bmatrix}_{in} \qquad \begin{bmatrix} V_{md} \\ I_{md} \\ V_{mc} \\ I_{mc} \end{bmatrix}_{out} = [P] \cdot [Mat] \cdot [P]^{-1} \cdot \begin{bmatrix} V_{md} \\ I_{md} \\ V_{mc} \\ I_{mc} \end{bmatrix}_{in}$$

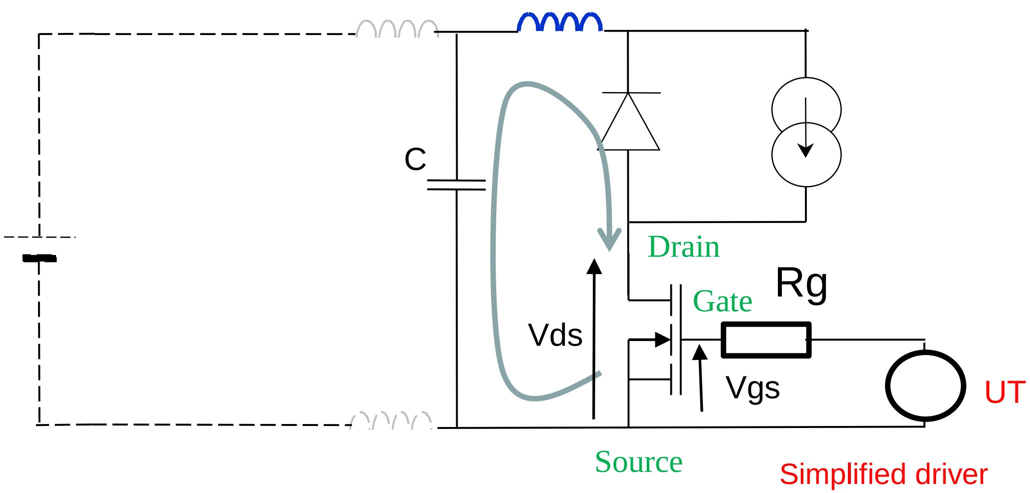
If Z2=Z3
And Z5=Z6

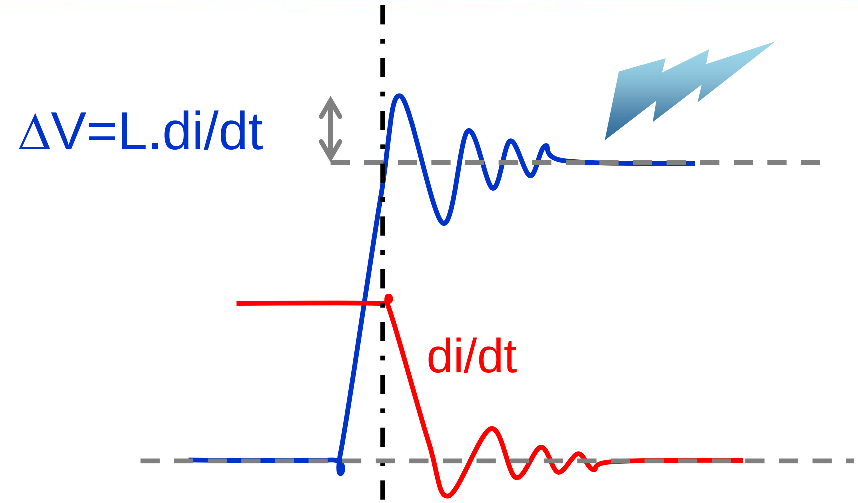
DM	0
0	CM

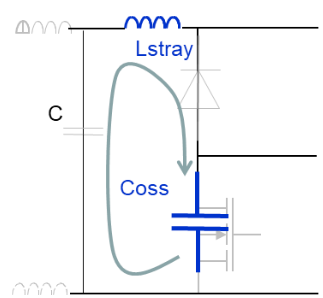
2. EMC & Semiconductor Packaging

- **Stray inductance:**
  Voltage overshoot & ringing

Stray inductance (switching loop)







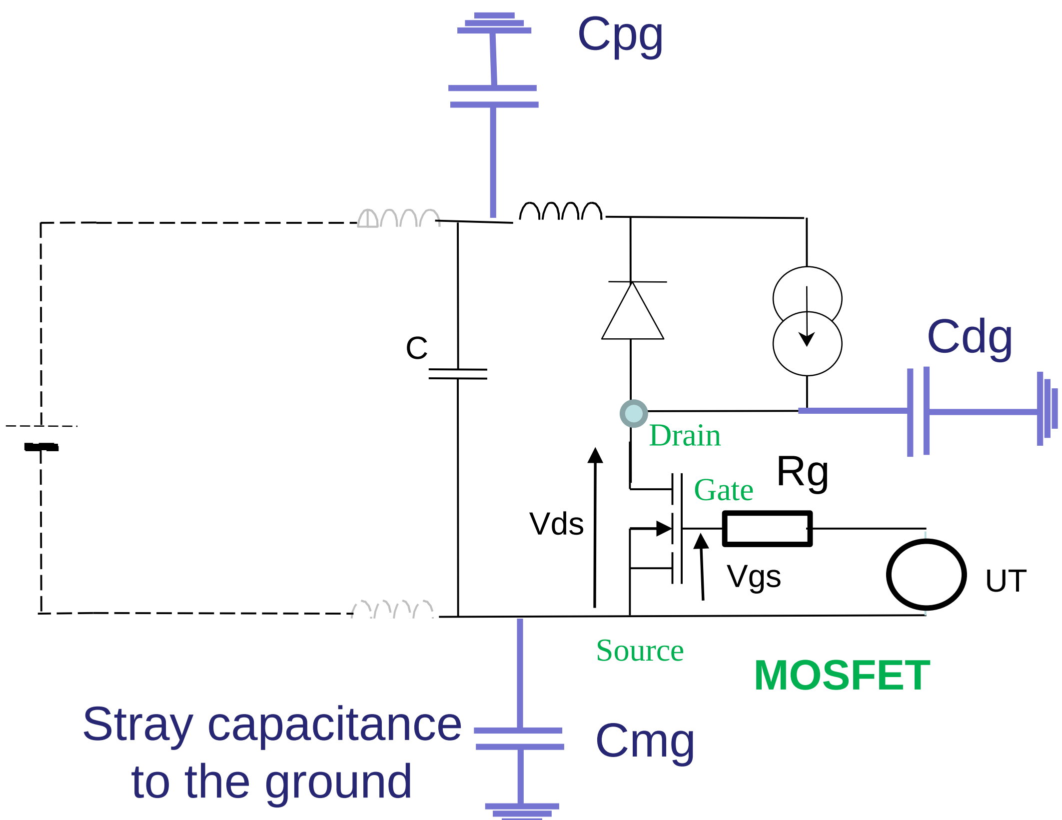
$$z = {}^{R}/_{2} \cdot \sqrt{{}^{Coss}/_{L_{stray}}}$$

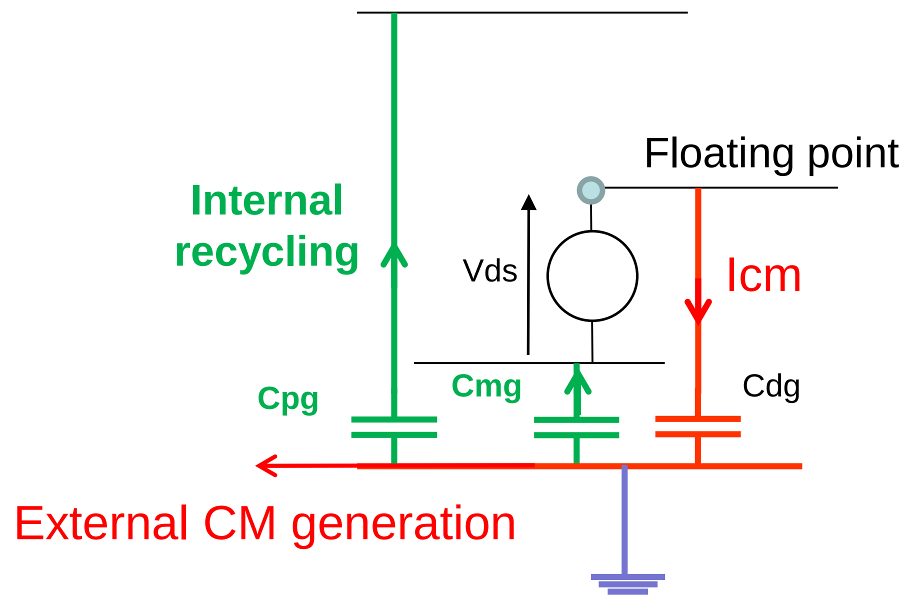
Reduced ΔV: 50A/ns*5nH → 250V!
Increased damping

Nano- or Subnano-henry requirements

2. EMC & Semiconductor Packaging

- **Stray capacitances & CM generation**





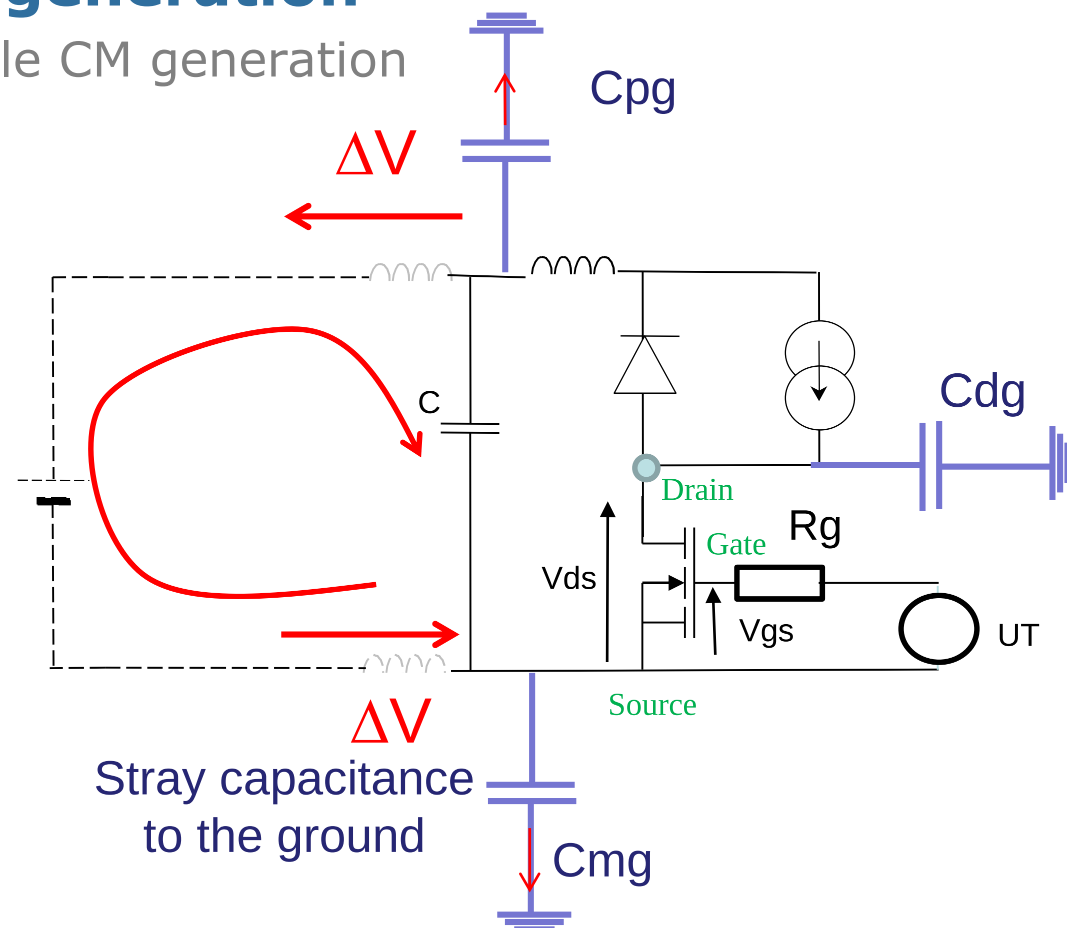
Reduce Cdg, increase Cpg, Cmg

2. EMC & Semiconductor Packaging

- **Stray capacitances & CM generation**
  - Warning: if Cpg ≠ Cmg: possible CM generation

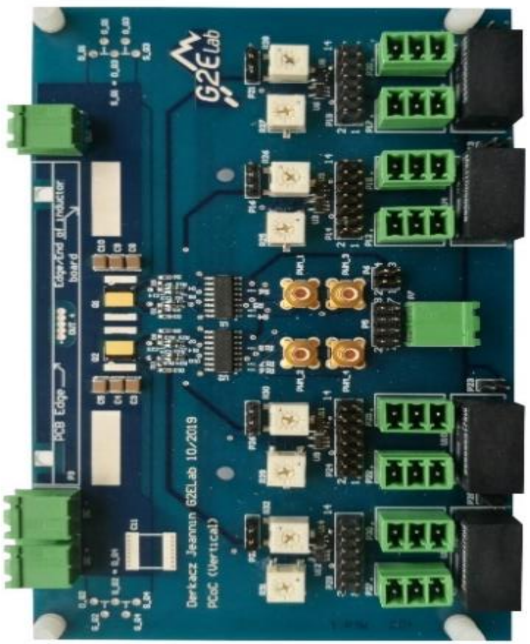
$$I_{Cpg} = Cpg\frac{d\Delta V}{dt} = -I_{Cmg}$$

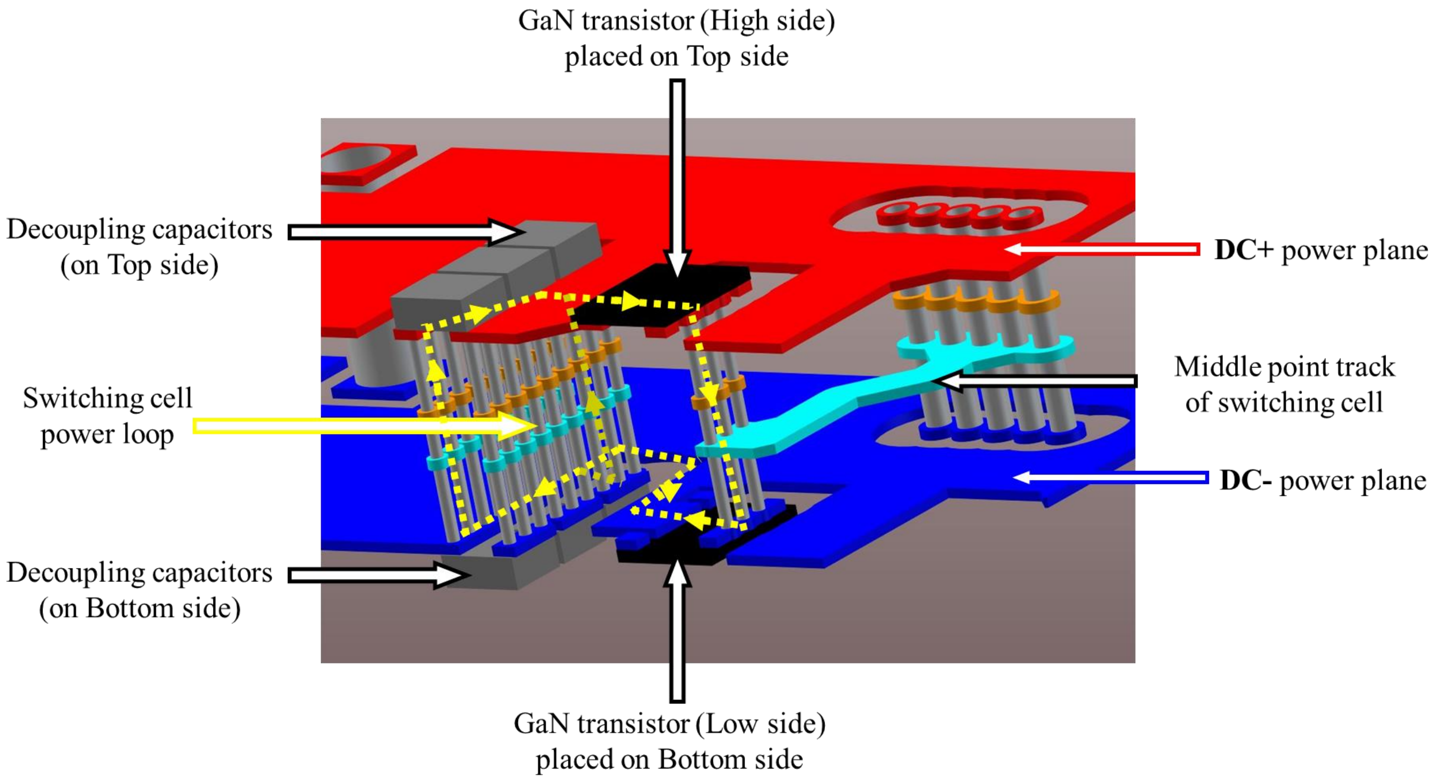
Only if Cpg=Cmg



Example of G2ELab recent result:

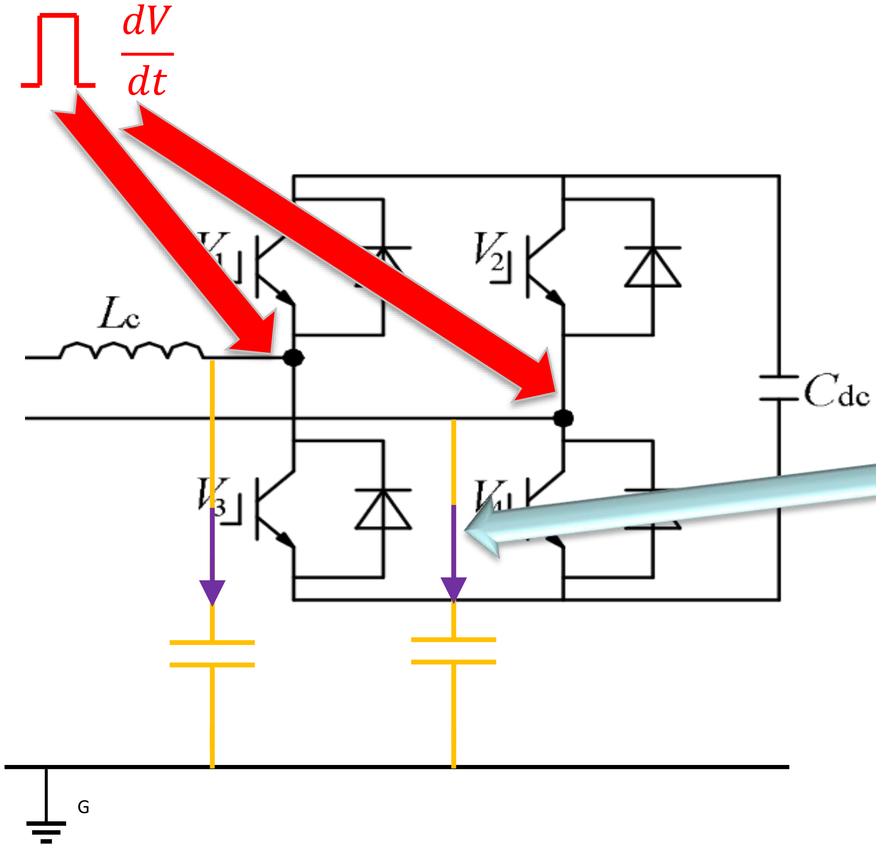
Power Chip on Chip applied to GaN devices





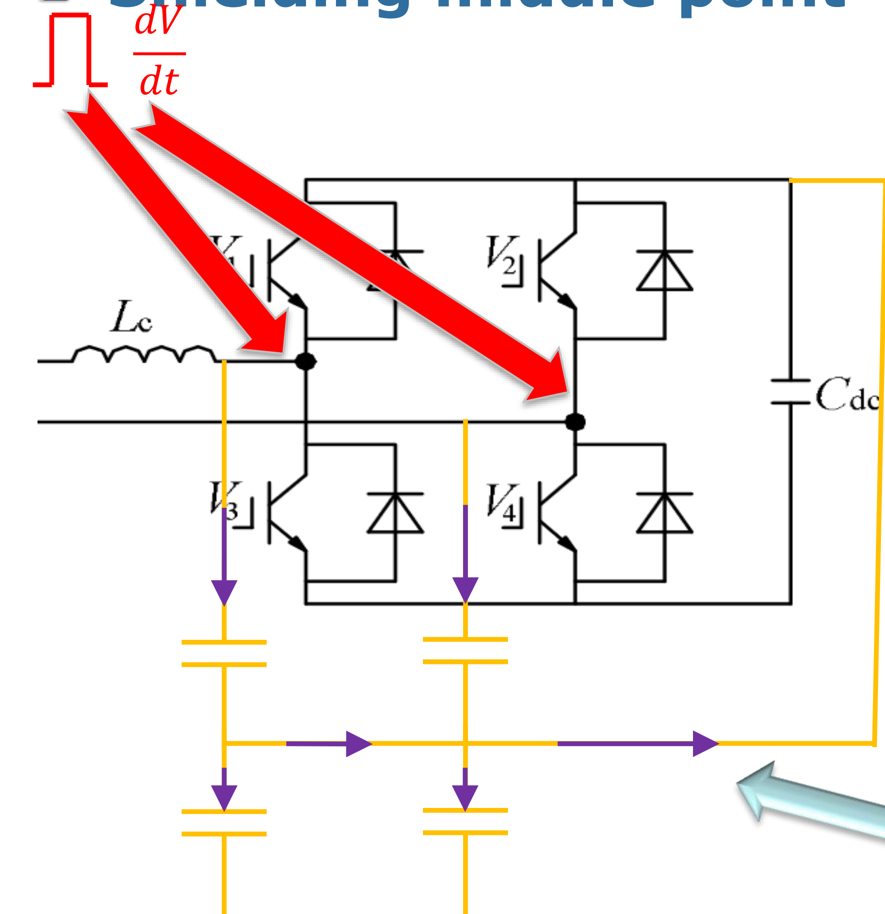
2. EMC & Semiconductor Packaging

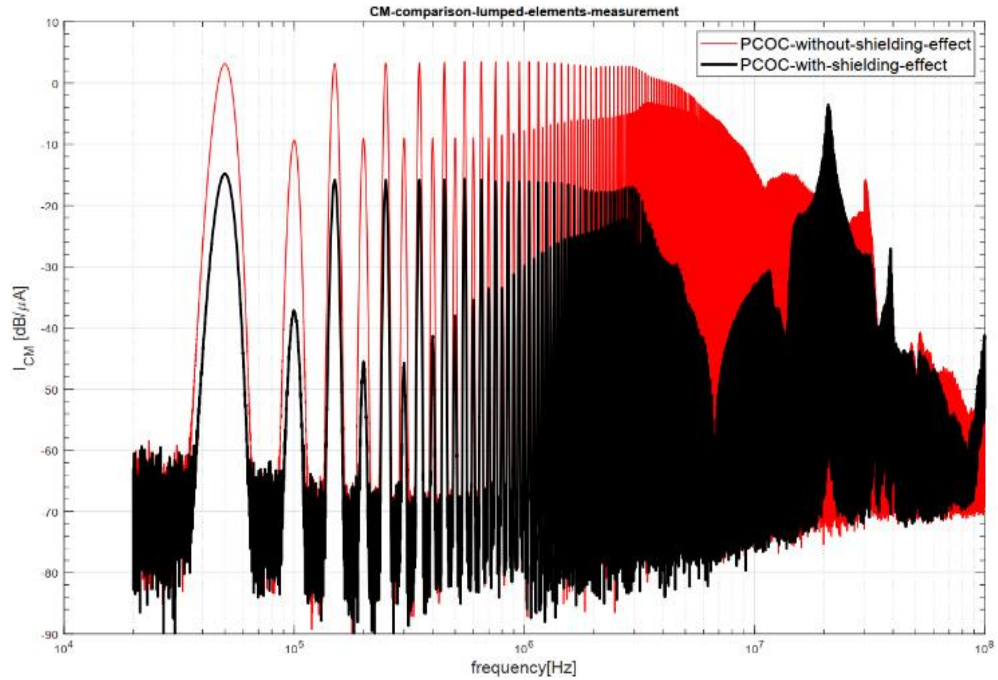
Shielding middle point



Huge Common Mode current generation!!!

Shielding middle point





Most of Common Mode current is recirculating inside converter

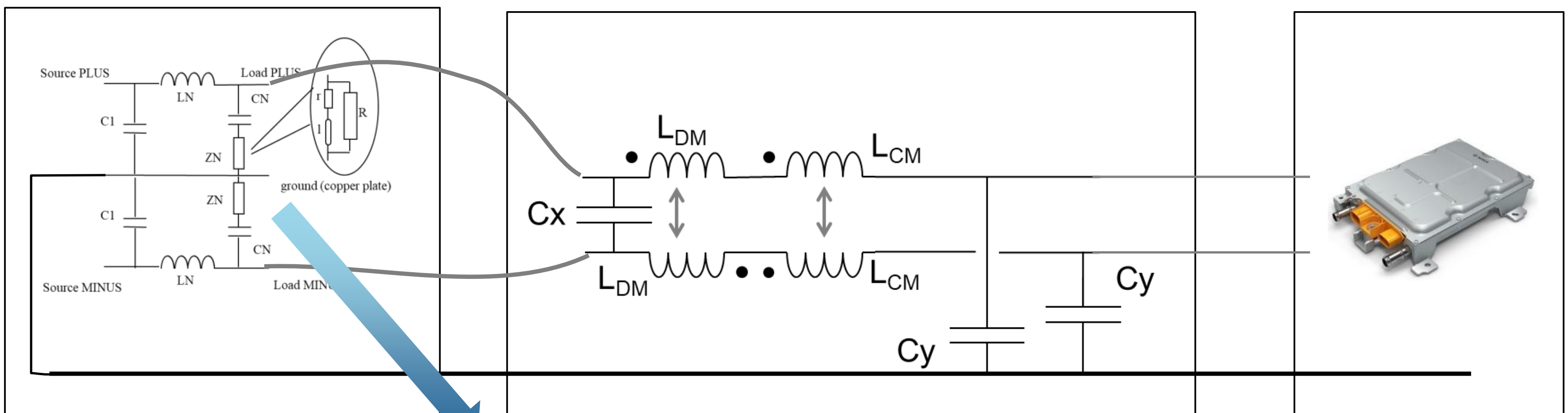
3. EMC Filter design and optimization

Design by optimization of EMC Filter

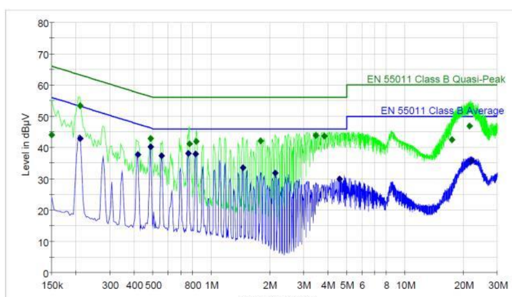
Normalized grid (LISN)

Filter (CM & DM)

converter

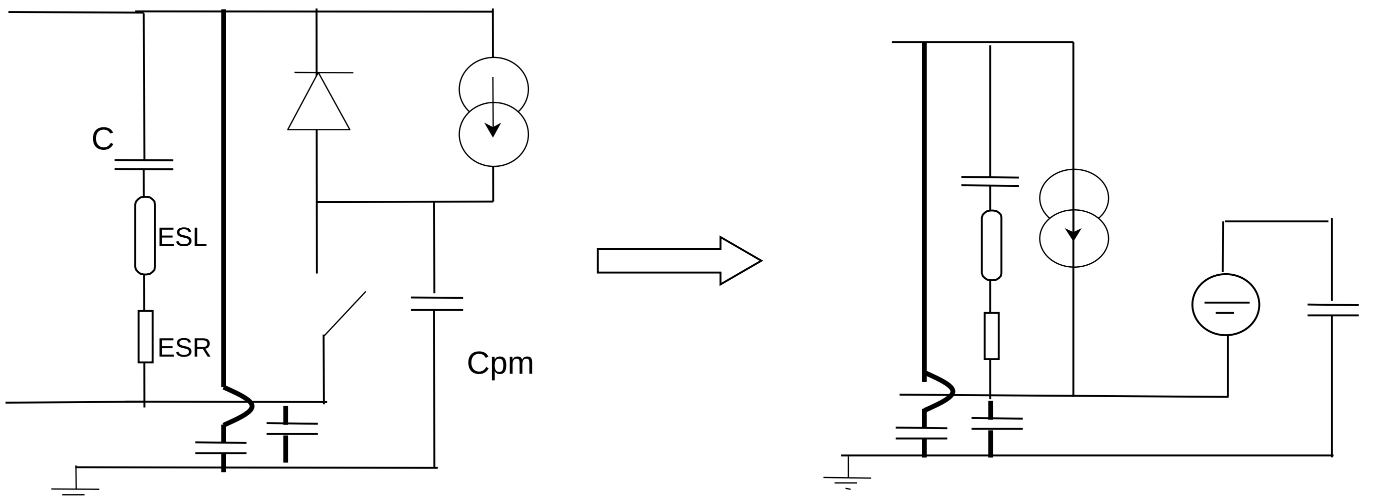


Line-Ground Voltage monitored



Design by optimization of EMC Filter:

Frequency model of the converter



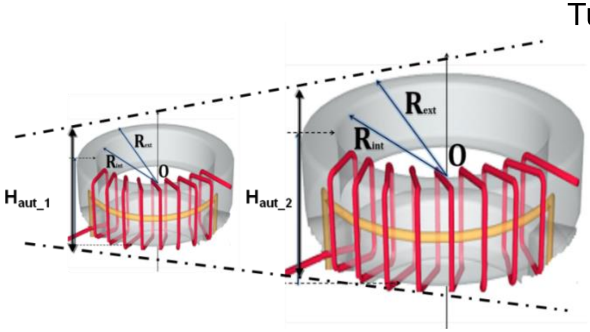
1 current source: current discontinuity
1 voltage source: voltage swing

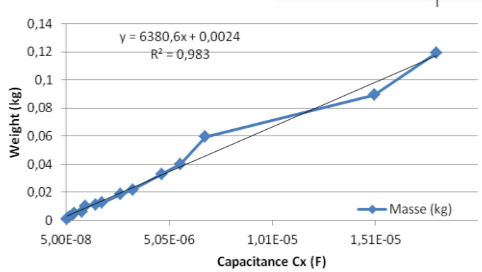
3. EMC Filter design and optimization

Design by optimization of EMC Filter:

Design Methodology

Turn number, core size, magnetic material





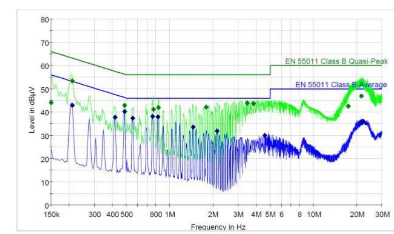
Datasheet interpolation
for capacitors

Converter Model

EMC Filter description

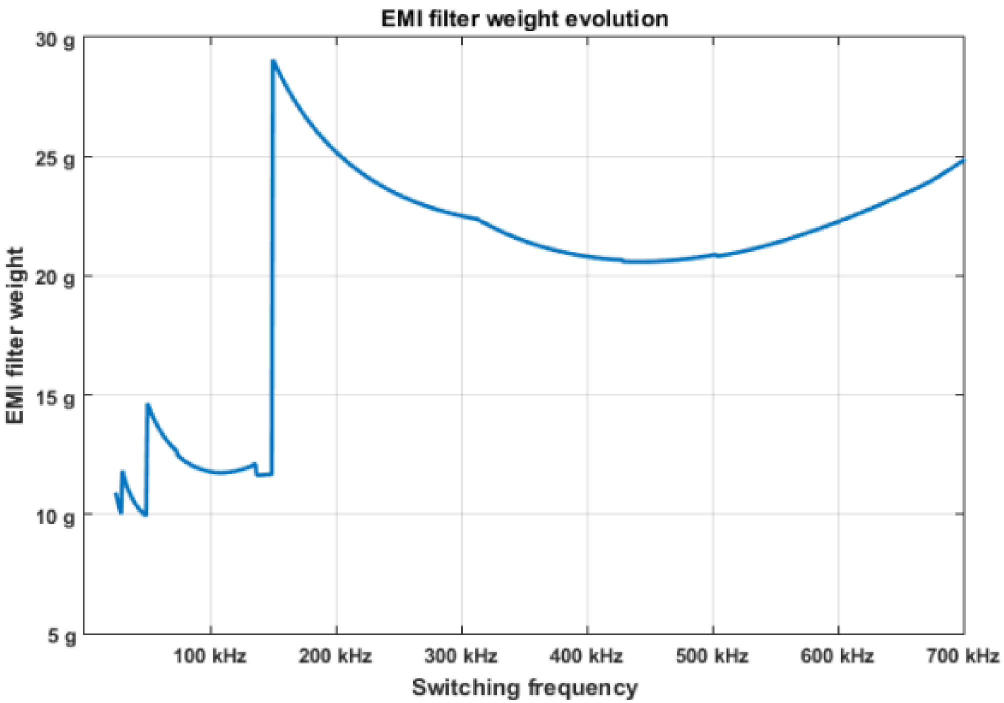
Constraints Evaluation
(Spectrum, stauration, losses, geometry, …)

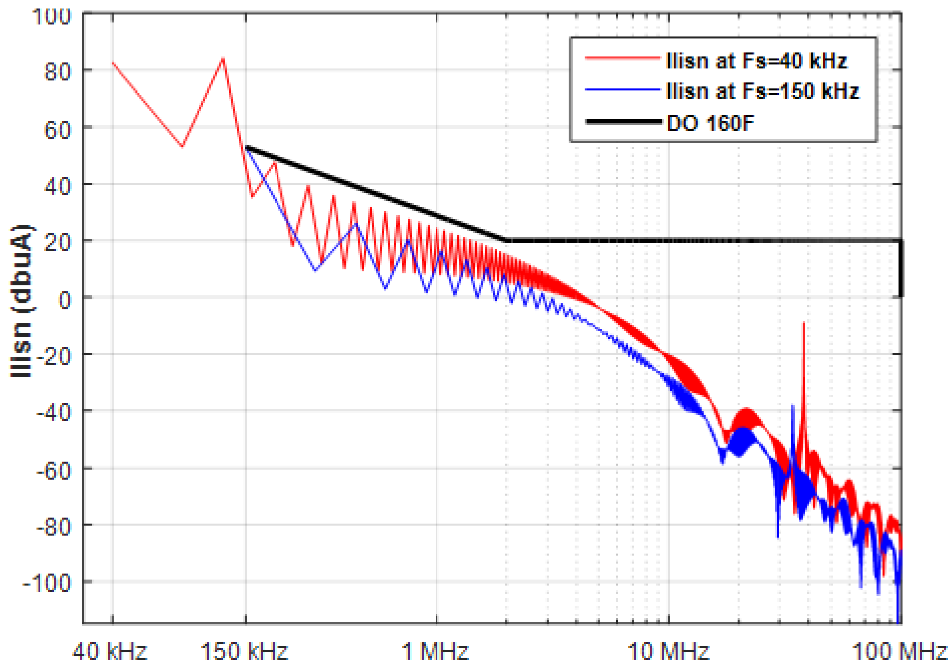
Mass evaluation



3. EMC Filter design and optimization

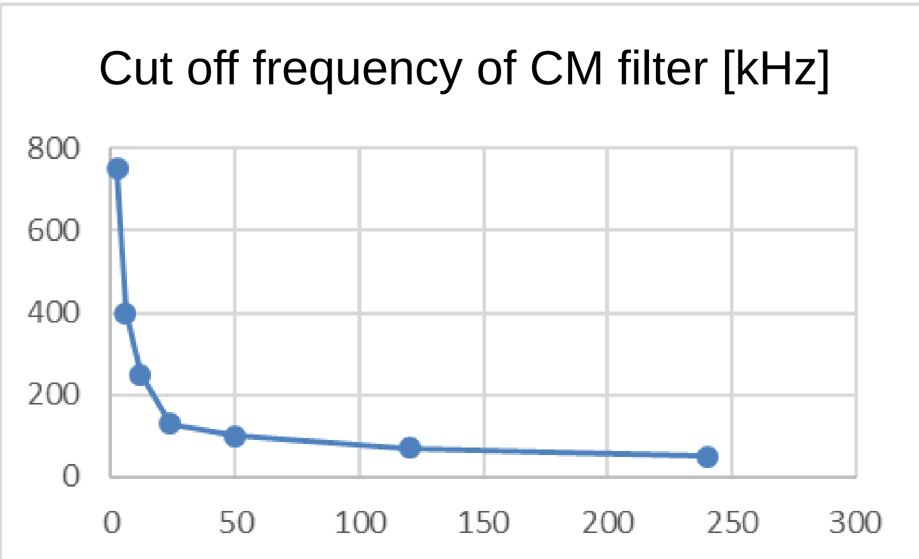
Design by optimization of EMC Filter: impact of Fsw



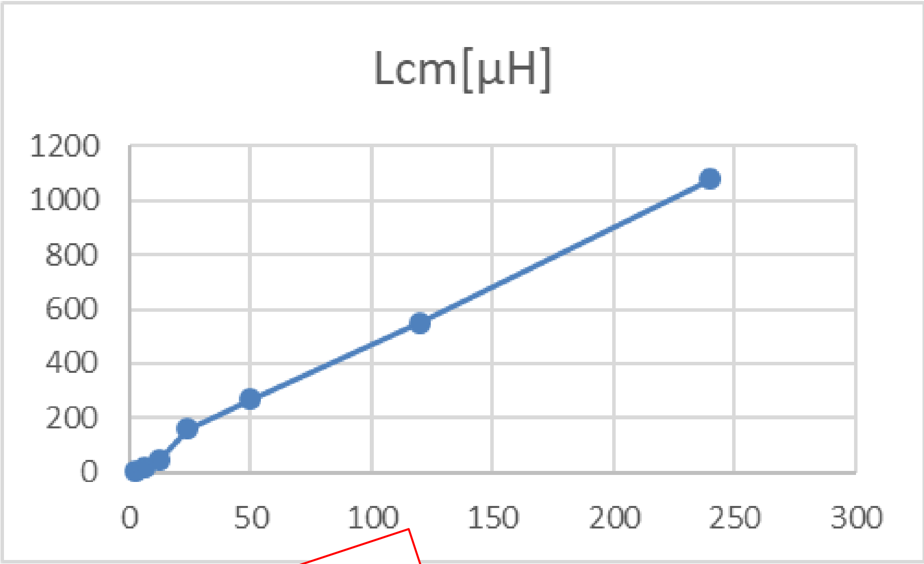


3. EMC Filter design and optimization

Design by optimization of EMC Filter: impact of floating point capacitance on the filter



Cpm[pF]

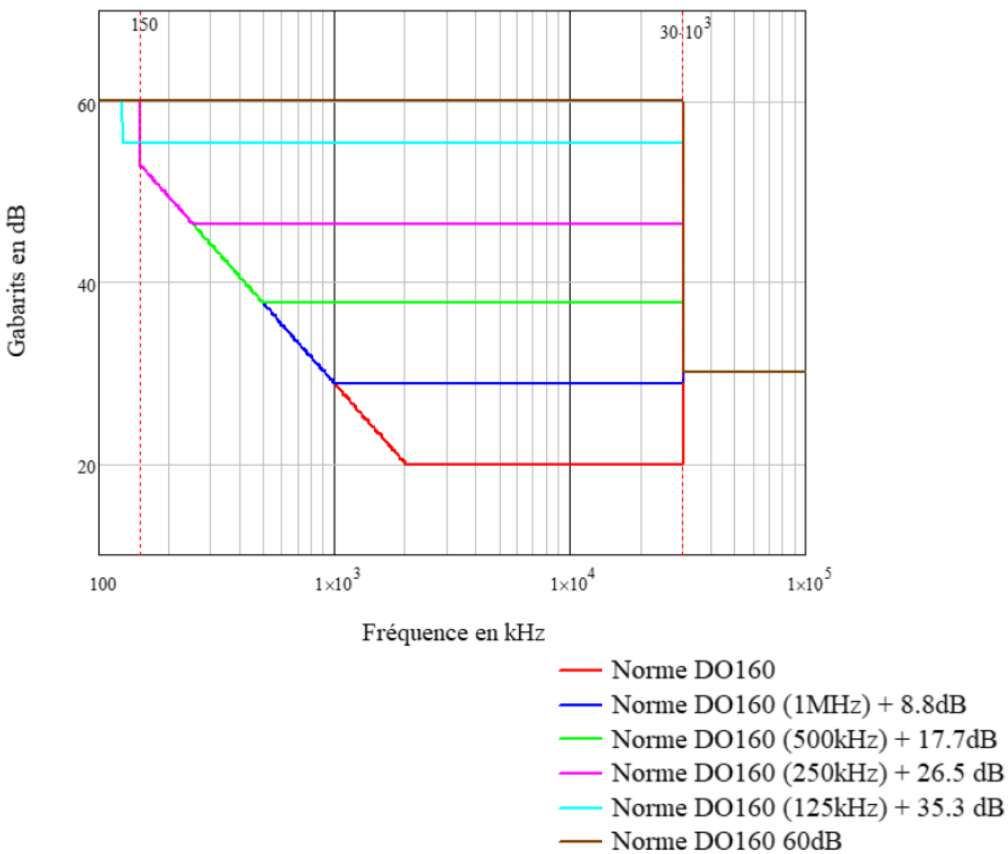


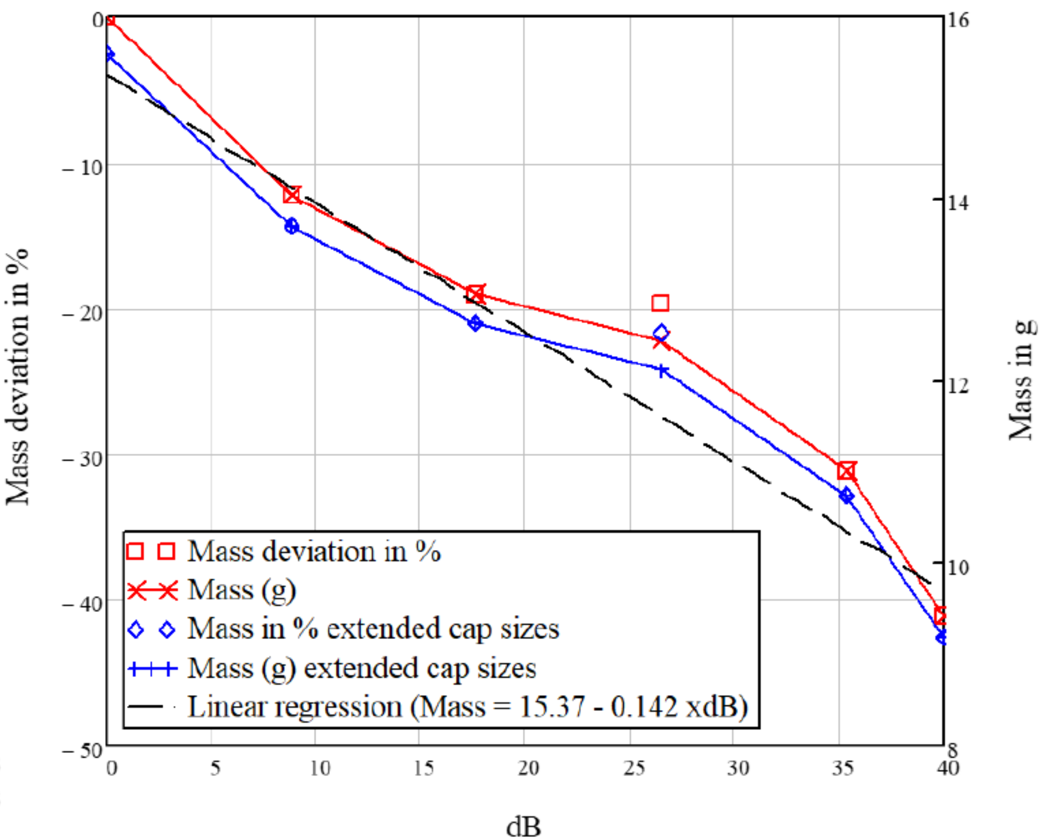
Cpm[pF]

Reducing EMI at packaging level

3. EMC Filter design and optimization

Variation of standard (DO160)

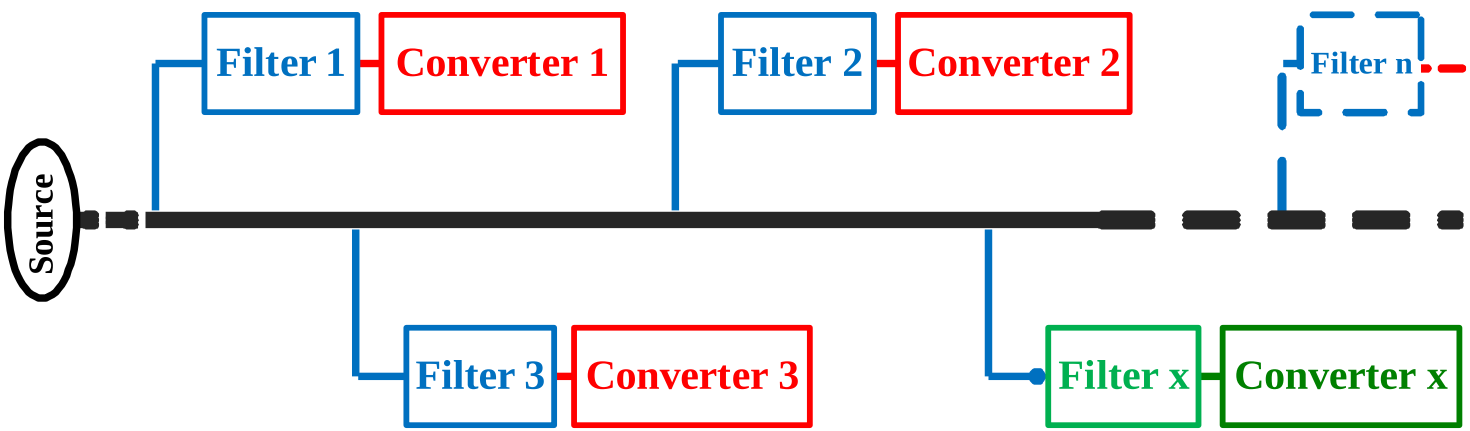




4. EMC models at system level

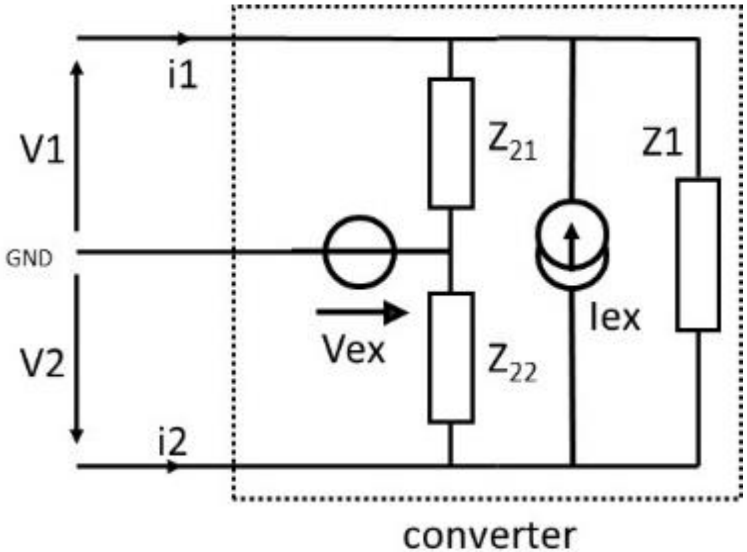
- **Usual EMC approach: standardized grid (LISN) and standardized emission level**
- **System optimization: real grids, computation of EMI level, comparison with disturbance level**

Need of EMC models at system level

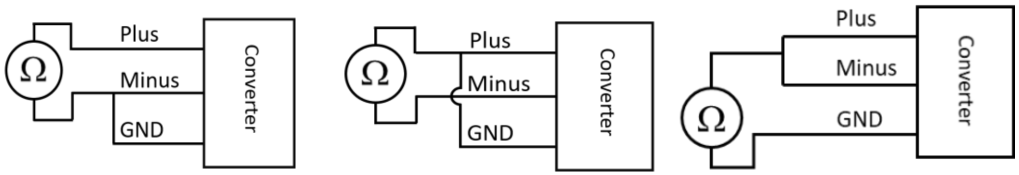


4. EMC models at system level

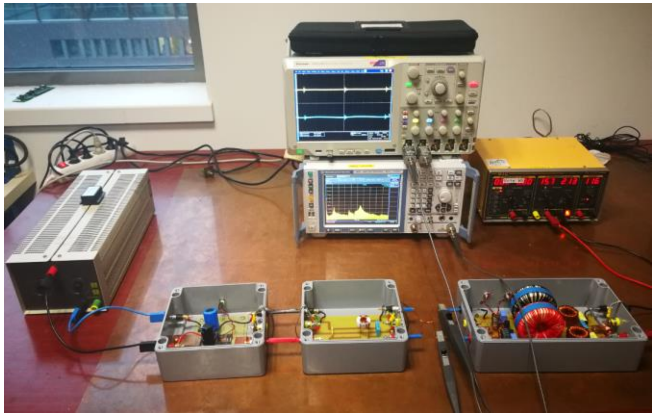
Black Box / Terminal Model



Identification process

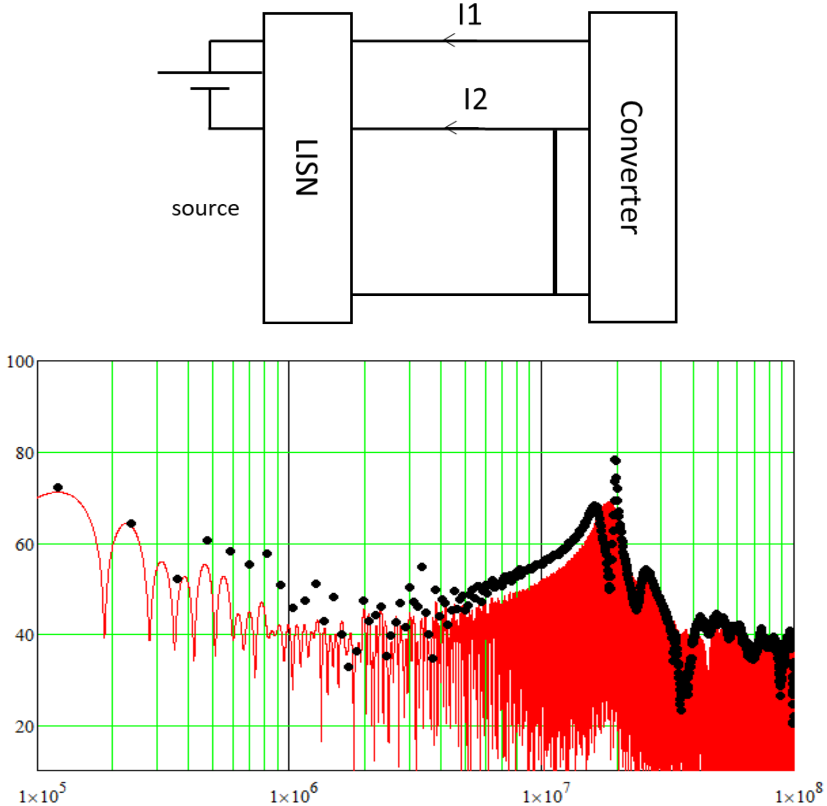


Off-line impedance measurement

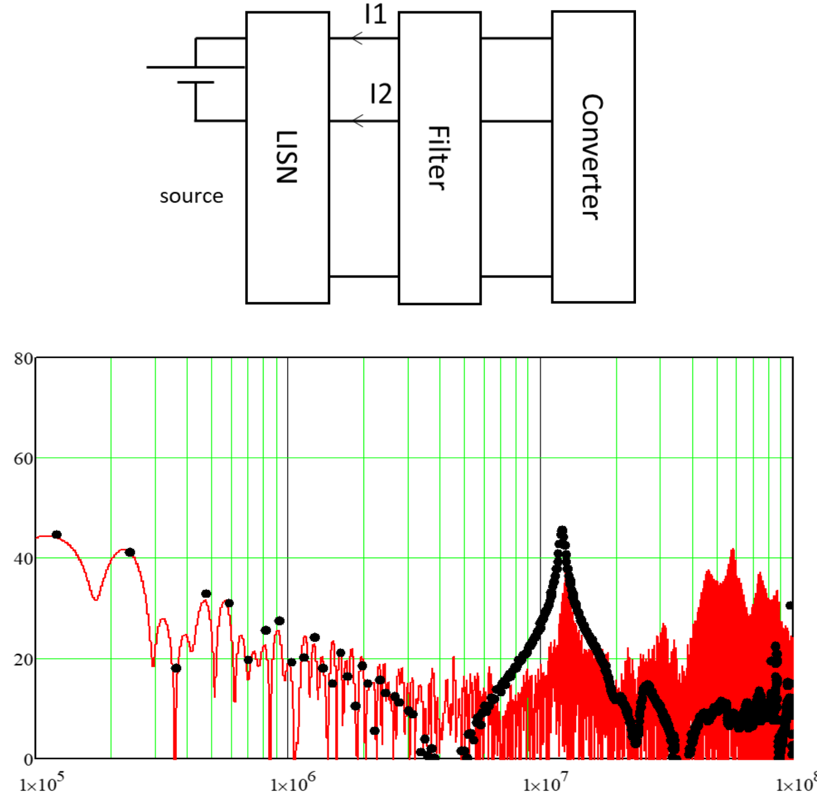


Line current measurement in a known configuration (LSIN)

Model validation in several configurations (exp results)



I1 – Minus to ground



I2 – EMC Filter

Conclusion

- **EMC as "dark side of Power Electronics"**
- **Wide Bandgap devices leads EMC issue more critical**
- **EMI reduction at packaging level**
  - Subnanohenry requirement
  - Reduced Floating Point capacitance, local shielding
  - Symmetry
- **EMC filter optimization**
  - Not straightforward phenomena
  - Technologically dependent
  - Proposed Design by Optimization methodology allows various studies (impact of technology, standards, …)
- **EMC model at system level**
  - Future challenge of embedded grids ?