Towards Wafer Scale Integration of CVD Graphene and 2D Materials

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Chair of Electronic Devices, RWTH Aachen University

AMO GmbH, Aachen

ImagineNano 2018

RWTH Aachen University & AMO GmbH

RWTH Aachen University

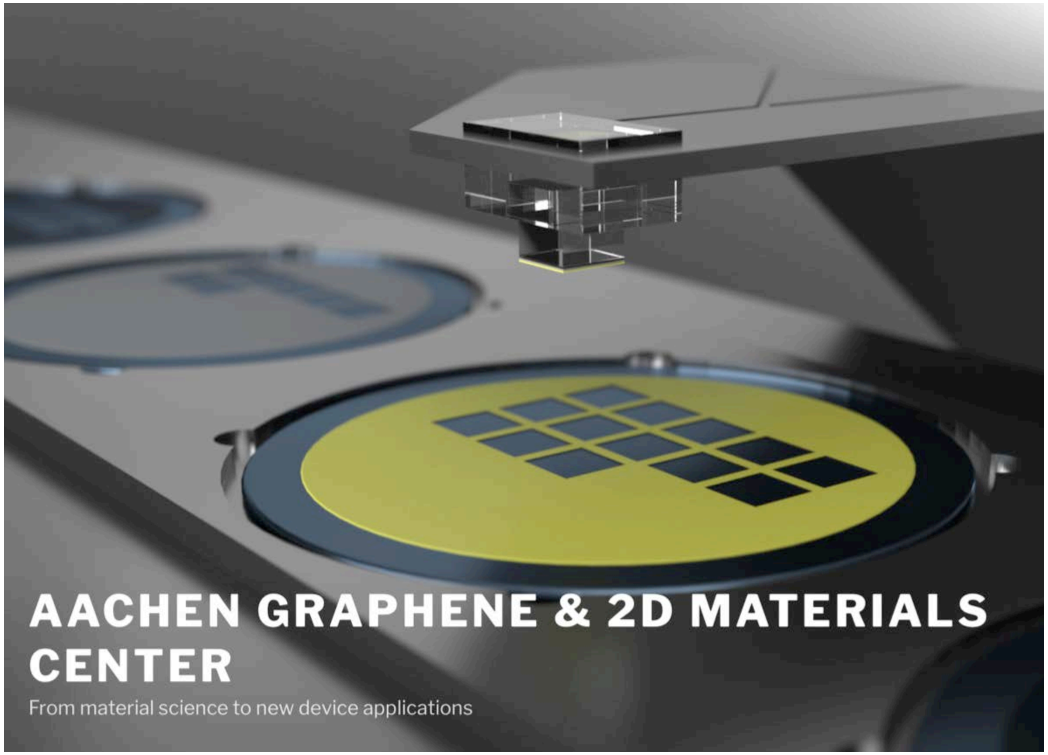
- Large European Technical Univ.
- 45.000 students
- Triangle:
  Germany / Belgium /Netherlands
- Chair of Electronic Devices (10)

AMO GmbH

- High-Tech SME / Institute (non-profit)
- Research Foundry
- 400 m^2 clean room
- 40 staff members

- Key technologies
  - Silicon Technology Base
  - Nanofabrication (NIL, E-Beam, IL)
  - New Materials Integration (high-k/metal gate, graphene, 2D)
  - Applications
    - Nanoelectronics
    - Nanophotonics
    - Integrated Sensors

Aachen Graphene and 2D Materials Center



Center founded in 07/2017

Members (7):
Prof. Christoph Stampfer (RWTH)
Prof. Joachim Knoch (RWTH)
Prof. Max Lemme (AMO and RWTH)
Prof. Markus Morgenstern (RWTH)
Prof. Renato Negra (RWTH)
Dr. Daniel Neumaier (AMO)
Prof. Andrei Vescan (RWTH)

→ Joint research activities
→ High-level seminars
→ Attract industry partners

Outline

- Introduction – Large Scale Growth
- Device Level Demonstration
- Integration & Metrology Challenges
- Wafer & System Scale Demonstrators

Chemical vapor deposition (CVD)

- Catalytic growth on Ni, Cu, Ru, Ir, TiC, Ta…

+ Process Temperatures: 850-1000°C

+ Transfer to random substrates

- Transfer process

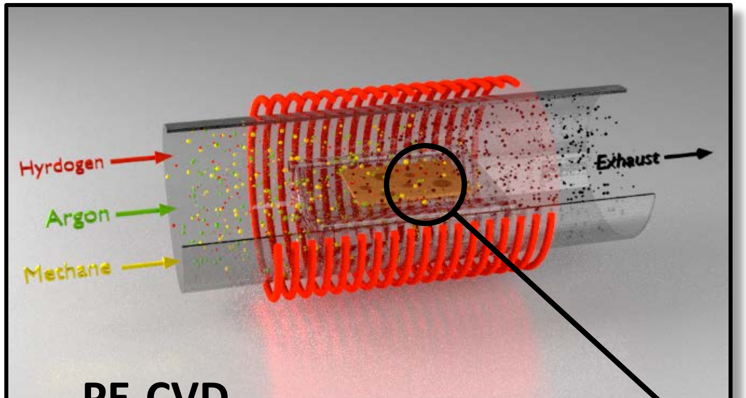
+ High potential for large areas (R2R)

- Monolayer vs. multilayer control (solubility)

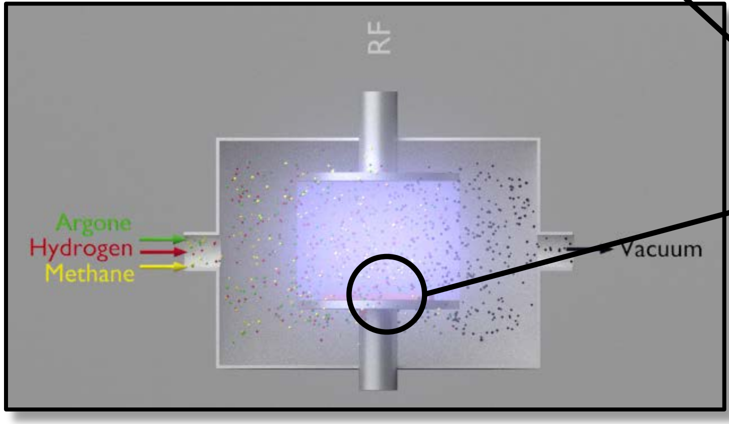
- Quality (grain boundaries, defects etc.)

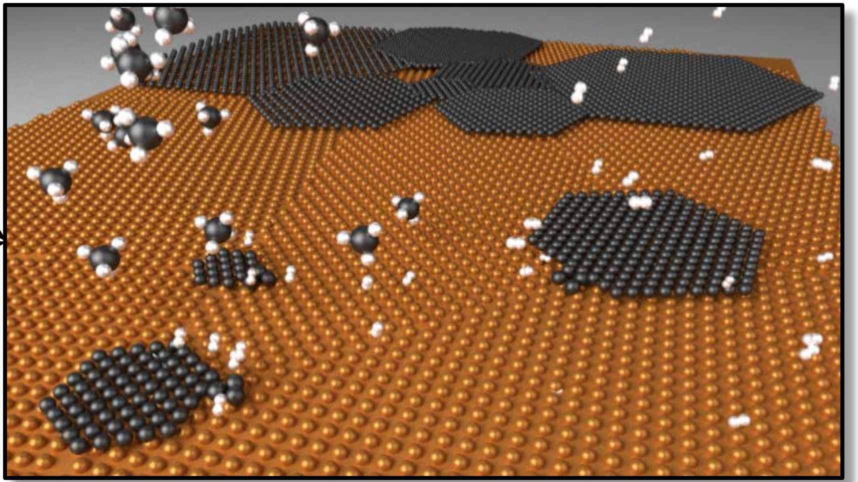
S. Kataria et al., physica status solidi (a), 2014., 2014

Thermal CVD



PE-CVD



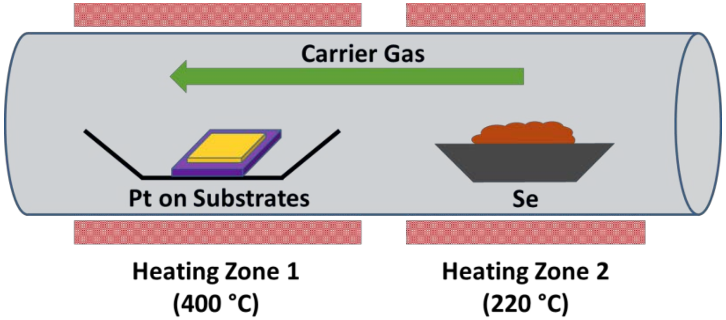


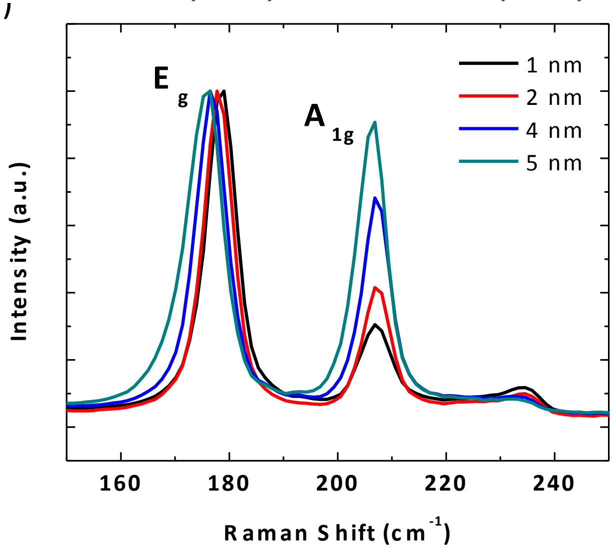
CVD process on copper substrate

Introduction: TMD Fabrication Methods

Example: $PtSe_2$

Thermally Assisted Conversion (TAC)

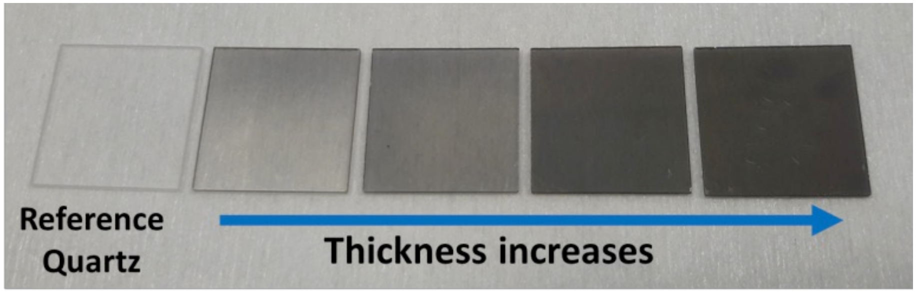




Collaboration with Prof. Georg Duesberg

- •Thermal conversion of metals (Pt, Mo, W, Pd,...)
- + Process Temperatures: 400 - 800°C
- **+ Growth on compatible substrates**
- - Monolayer vs. multilayer control (solubility)
- - Quality (grain boundaries, defects etc.)

Universität der Bundeswehr München



Yim *et al*., ACS Nano, 2016
Yim *et al*., Nano Letters, 2018

Introduction: Graphene Fabrication Methods

Wafer scale

Rahimi et al. ACS Nano (2014)

Roll-to-Roll Production

Fabrication, Characterisation and Applications of 2D-Nanomaterials

HEA2D

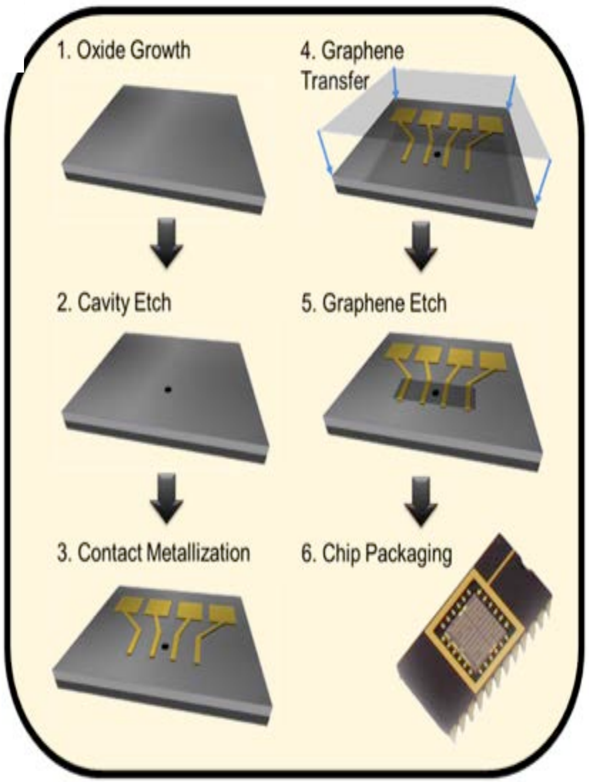
- RWTH Aachen
- Uni Duisburg
- Aixtron
- Coatema
- Fraunhofer IPT

EUROPÄISCHE UNION
Investition in unsere Zukunft
Europäischer Fonds
für regionale Entwicklung

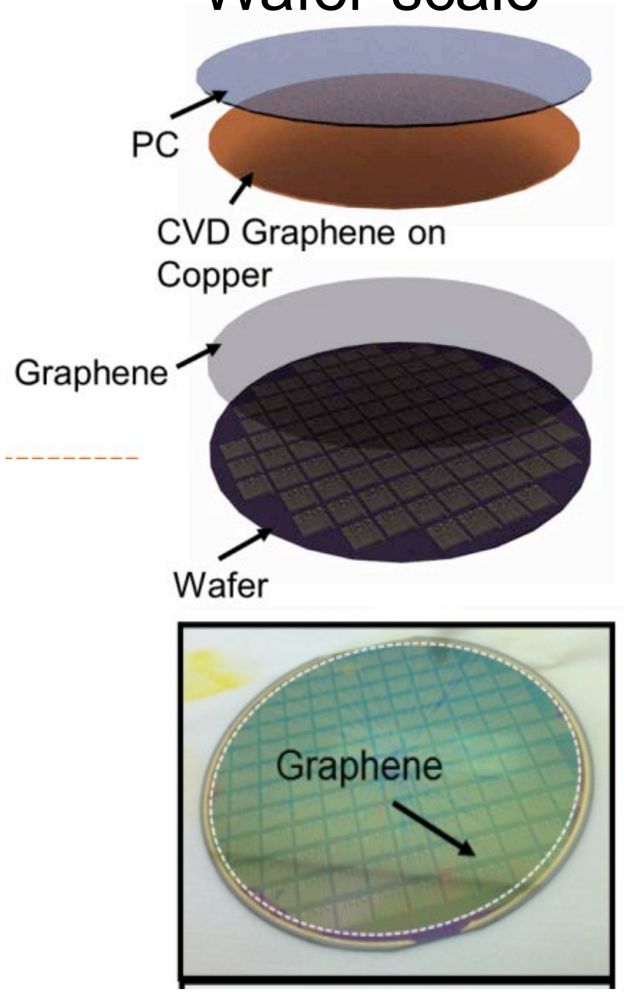
EFRE.NRW
Investitionen in Wachstum
und Beschäftigung

Introduction: Graphene Fabrication Methods

Chip-scale

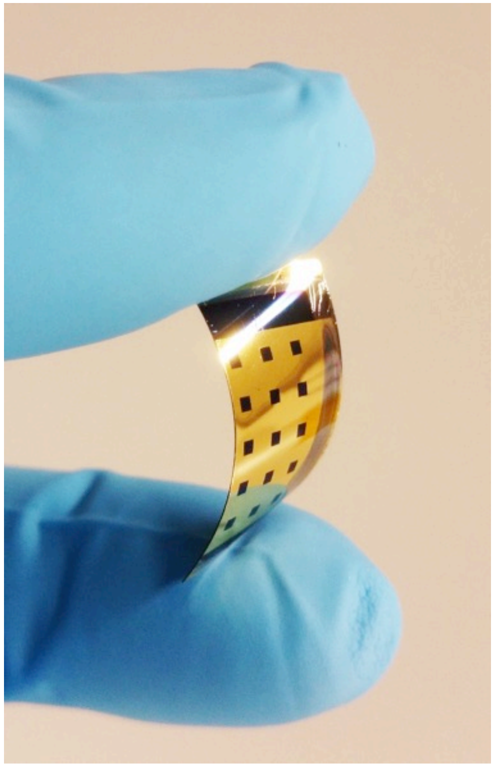


Wafer-scale



Smith et al, Sol. St. Electr., 2015
Smith et al., IEEE TED, 2017

Flexible



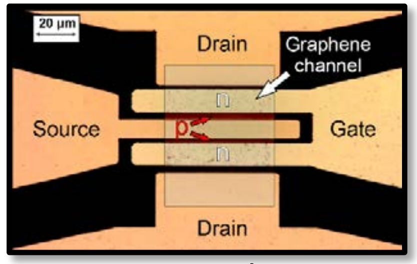
Schneider *et al.*, Nanoscale, 2017

Introduction: Device Research @ RWTH & AMO

Exploit 2D Material properties in electronic devices

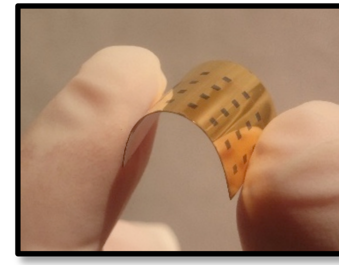
- Mono atomic layers
- Highly conductive
- Optical transparency of 97.7%
- Young‘s modulus: 1 TPa
- Stretchability: up to 20%
- …

Electronics



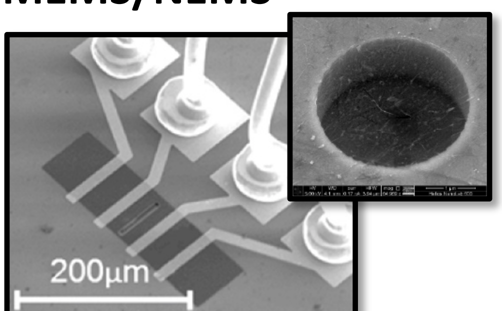
Graphene / TMD transistors

Flexible electronics



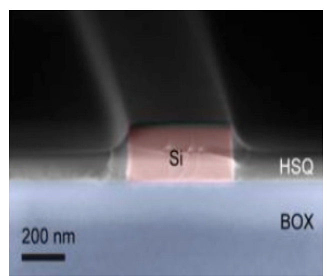
Photodetectors
Hall sensors

MEMS/NEMS

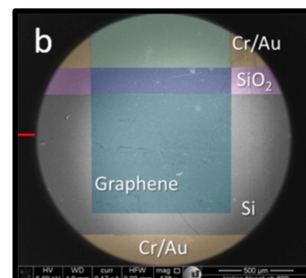


Graphene & TMD pressure & gas sensors

Optoelectronics

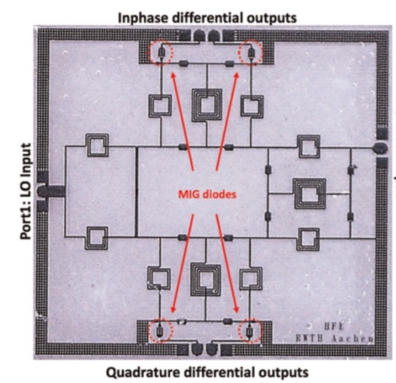


Graphene/Si photonics



Graphene/Si & TMD/Si photodetectors

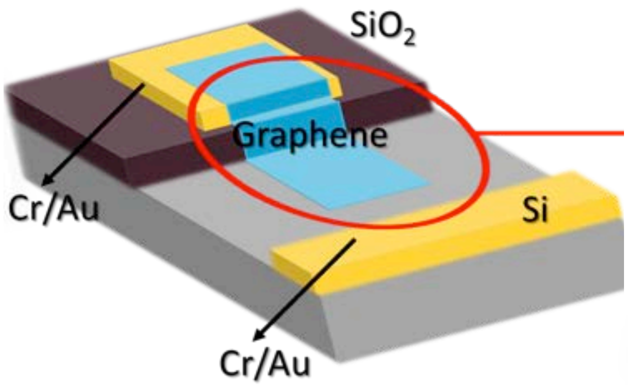
Integrated circuits



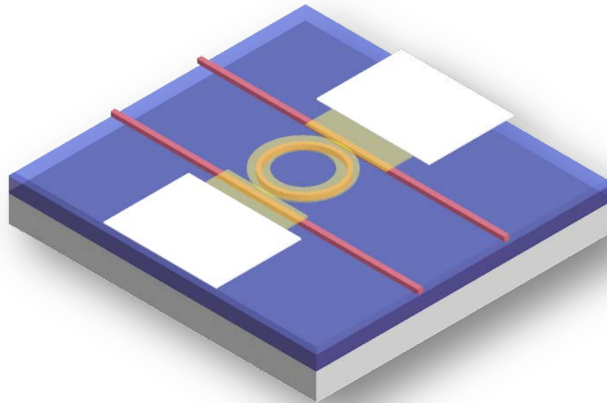
Six port receiver (design: Negra group)

Graphene / Silicon Photonics Integration

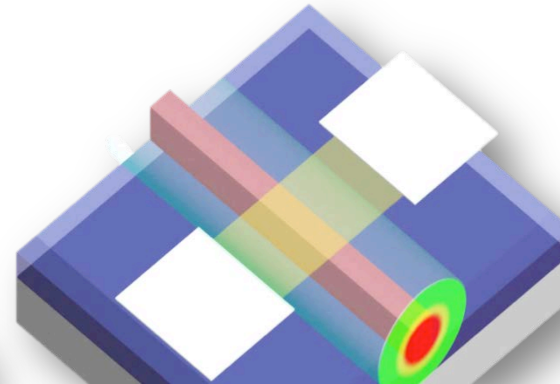
G / si diodes: R > 600 mA/W



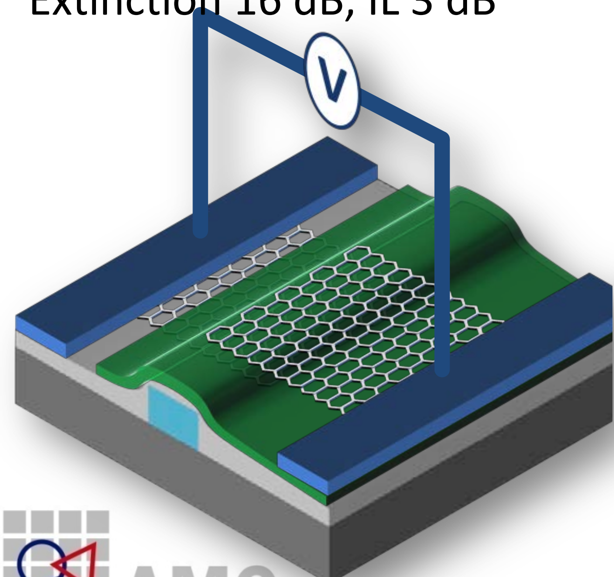
Phase modulator: $V_{\pi}L\alpha$ = 14 dBV



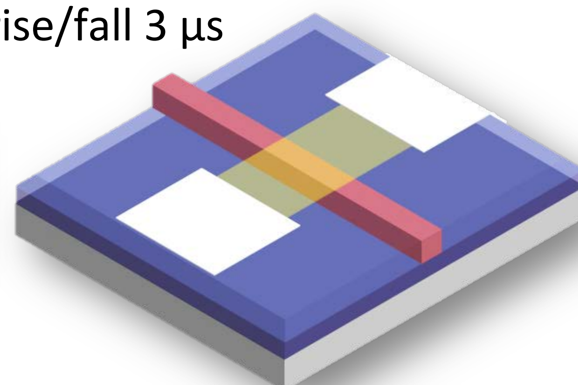
Photodetector: 130 GHz, 0.2 A/W



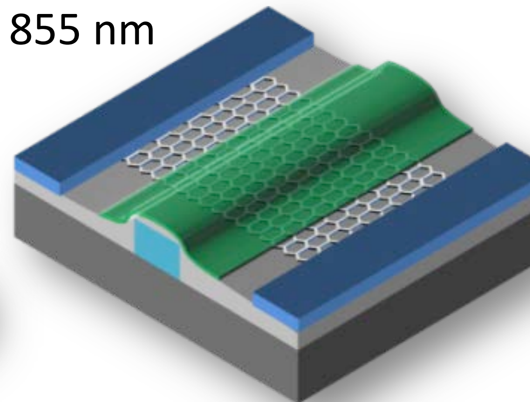
Absorption modulator:
Extinction 16 dB, IL 3 dB



Heater: 0.3 nm/mW
rise/fall 3 µs



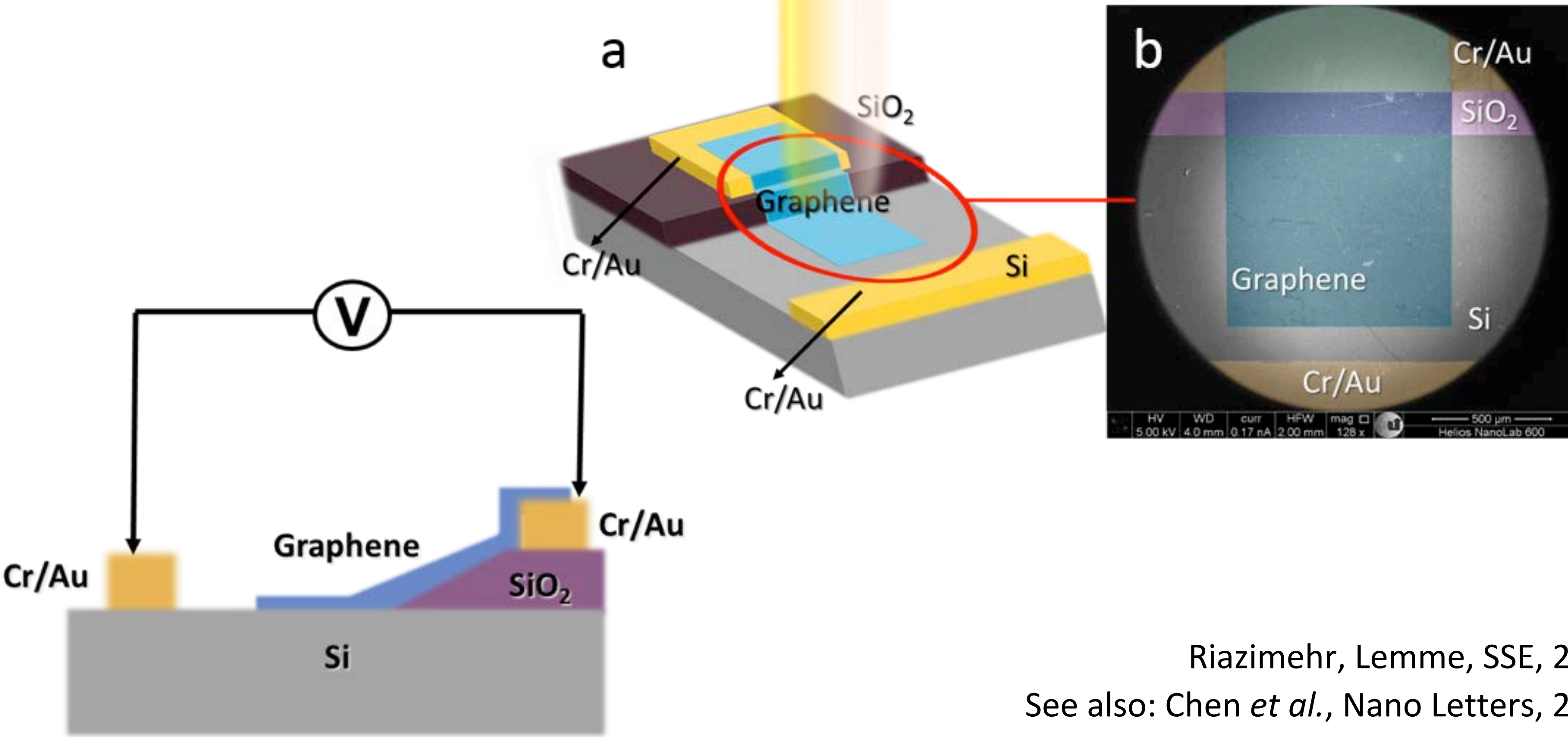
Variable Optical Attenuator
@ 855 nm



Graphene / Silicon Photodetectors

2D/3D cointegration of graphene/silicon photodetectors

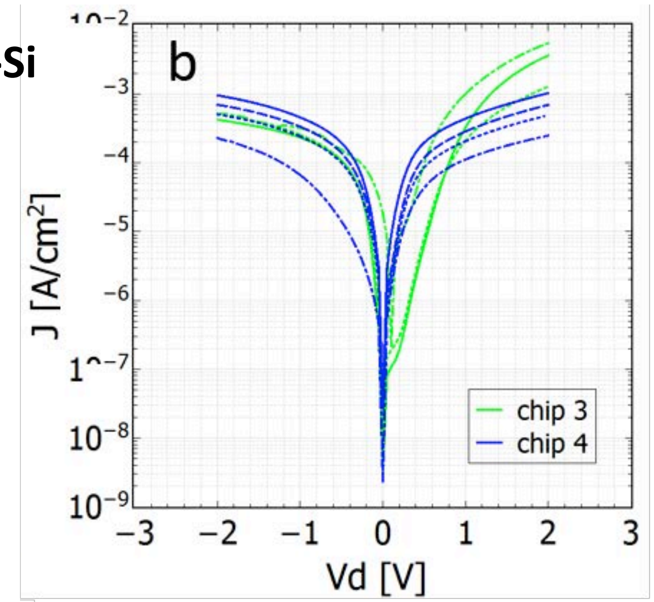
- Vertical device architecture

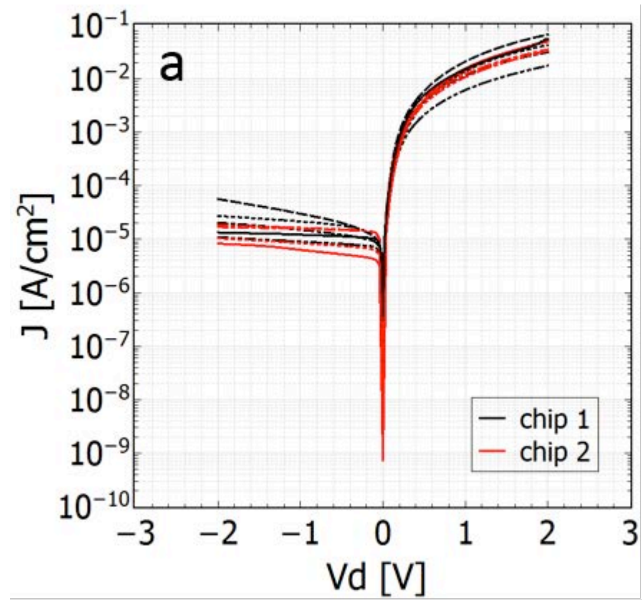


Riazimehr, Lemme, SSE, 2016
See also: Chen *et al.*, Nano Letters, 2011
An *et al.*, Nano Letters, 2013

Graphene / Silicon Photodetectors

Graphene/p-Si



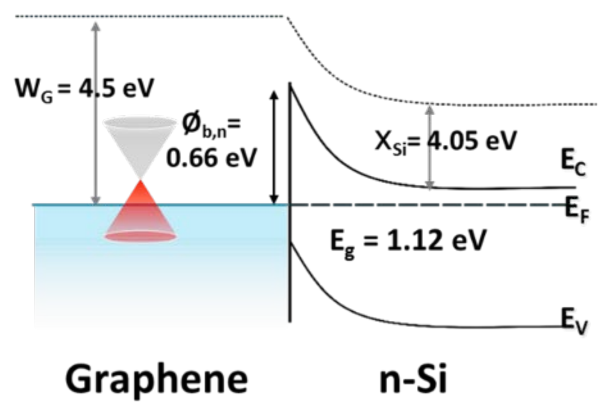


Graphene/n-Si

- Shockley equation:

$$I = I_S[\exp\left(\frac{qV_d}{nk_BT}\right) - 1]$$

  - Ideality factor n =1.52
  - Barrier height $\O_b$ =0.66 eV
- p doping due to exposure to ambient atmosphere

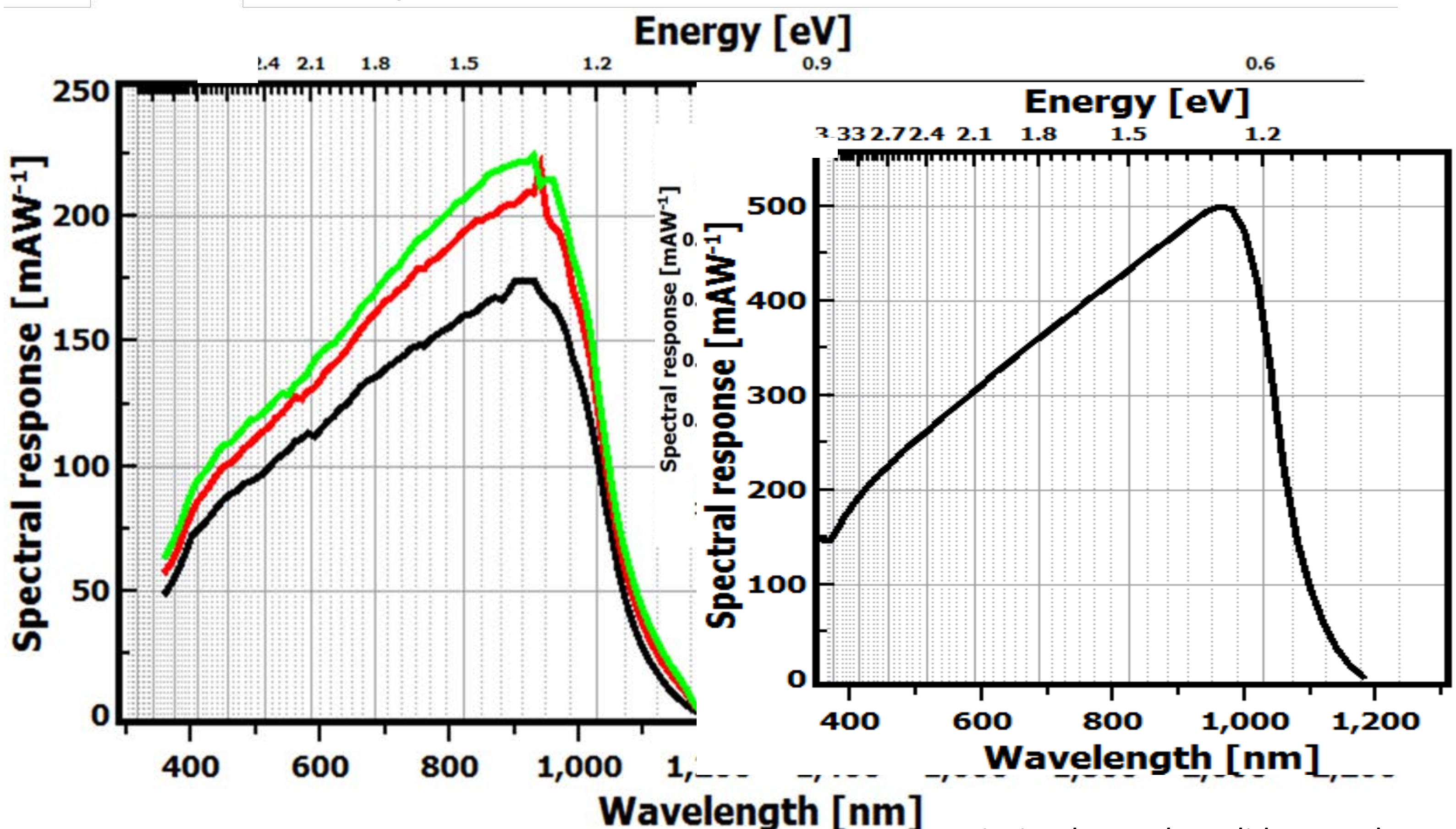


Riazimehr *et al.*,, Solid State Electronics, 2016

Spectral Response

Graphene/ n-Si photodiode

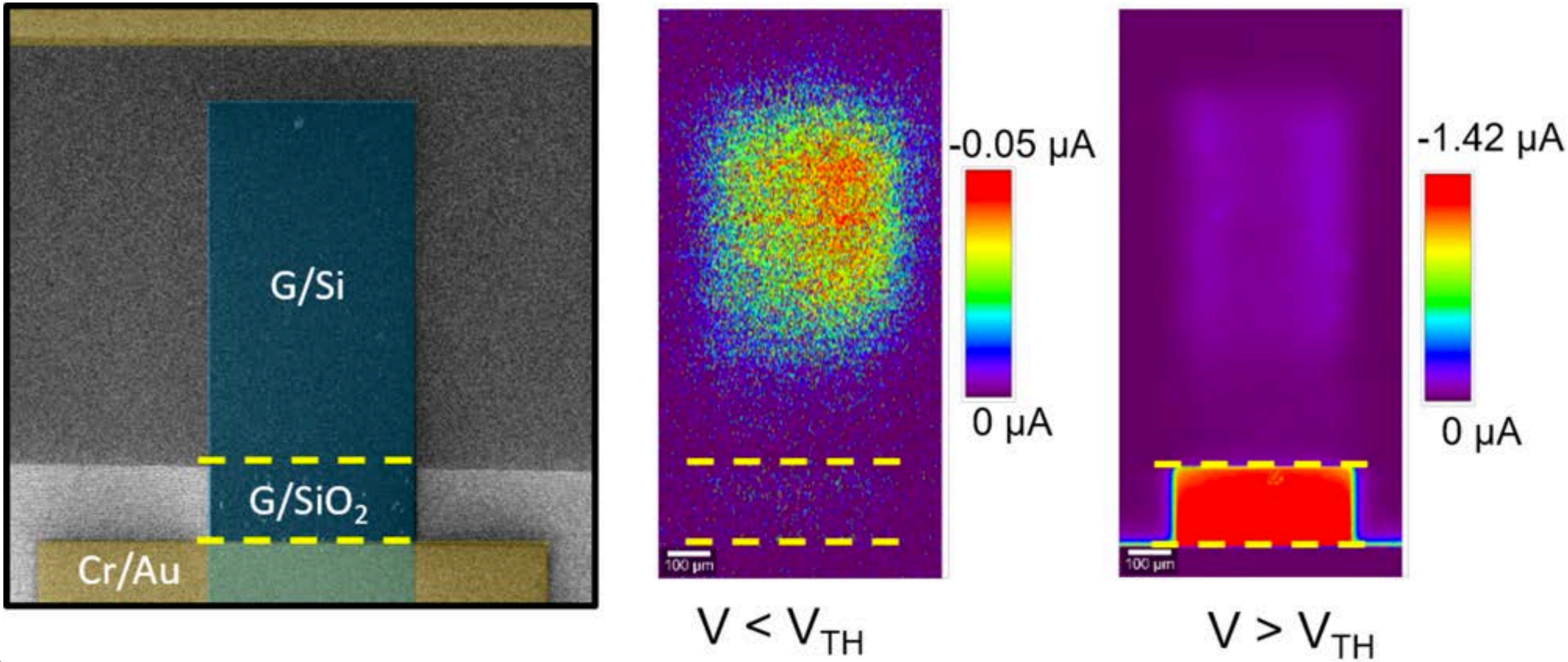
Calibrated Si photodiode



Riazimehr *et al.*,, Solid State Electronics, 2016

Spectral Response

Optimized graphene/ n-Si photodiode



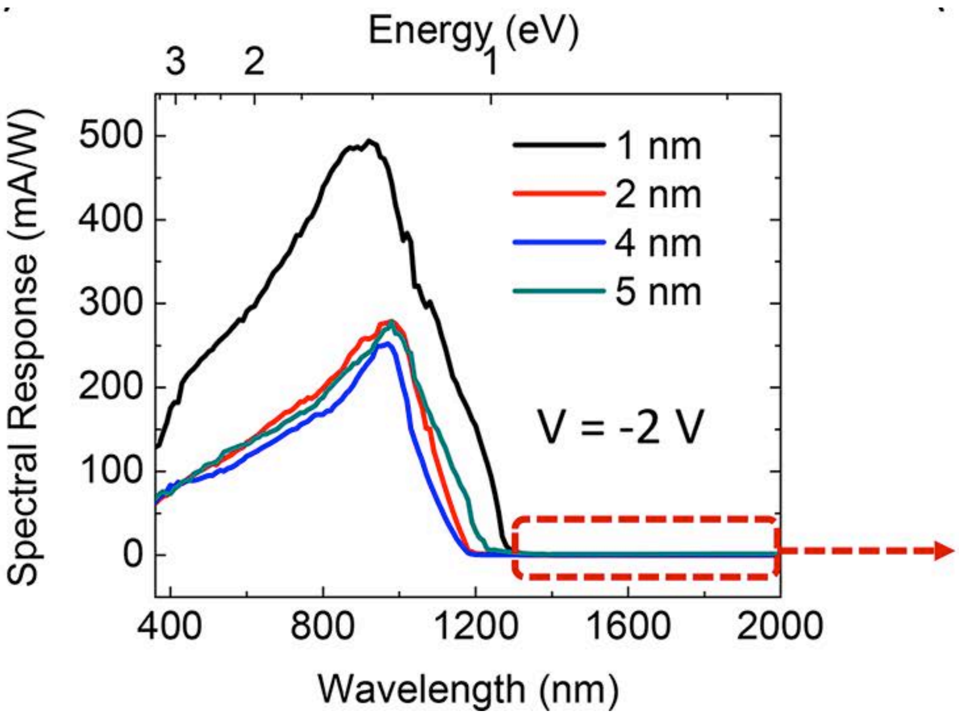
Riazimehr et al., ACS Photonics, 2017

Riazimehr *et al.*, in preparation, 2018

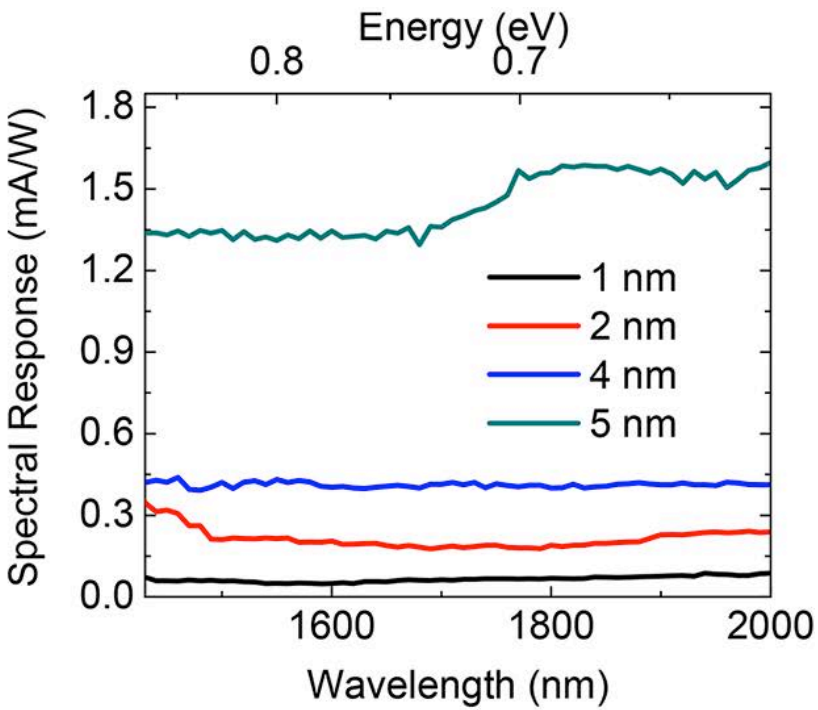
PtSe$_2$ / Silicon Photodetectors

Spectral Response

PtSe$_2$/ n-Si photodiode



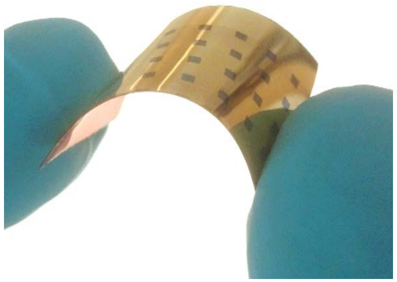
Infrared sensitivity

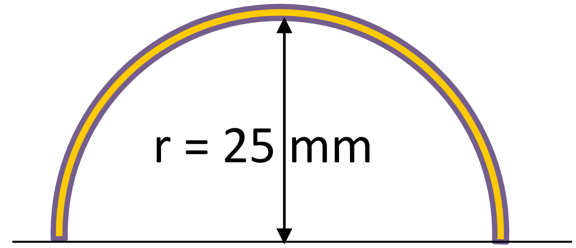


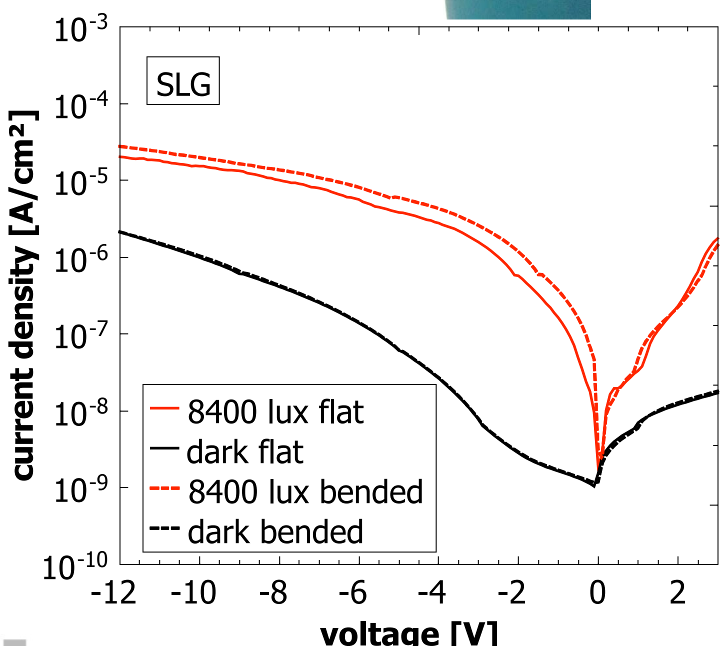
Yim *et al.*, Nano Letters, 2018

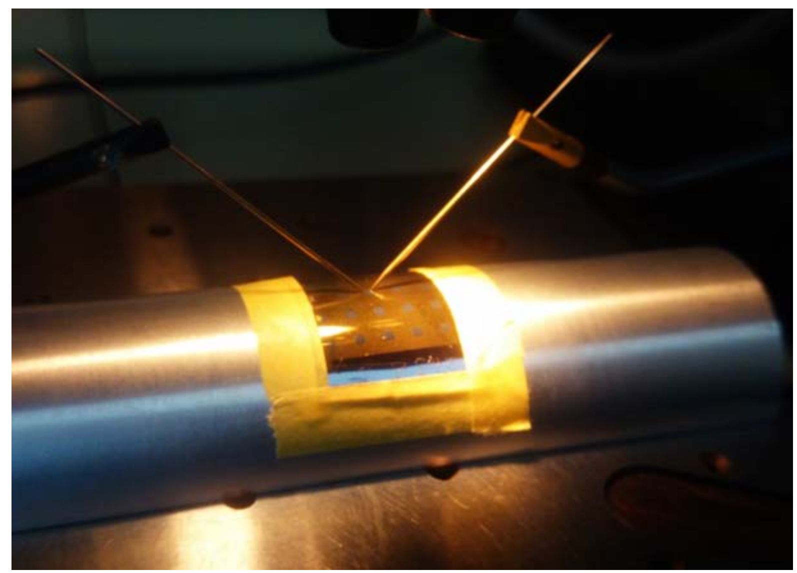
Yim *et al.*, *NPJ* 2D Materials and Applications, 2018

Bendable & flexible graphene / a-Si:H photodetectors





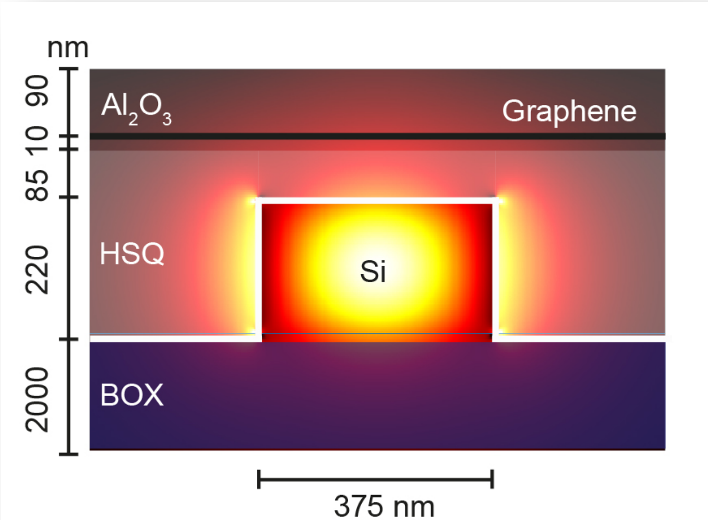


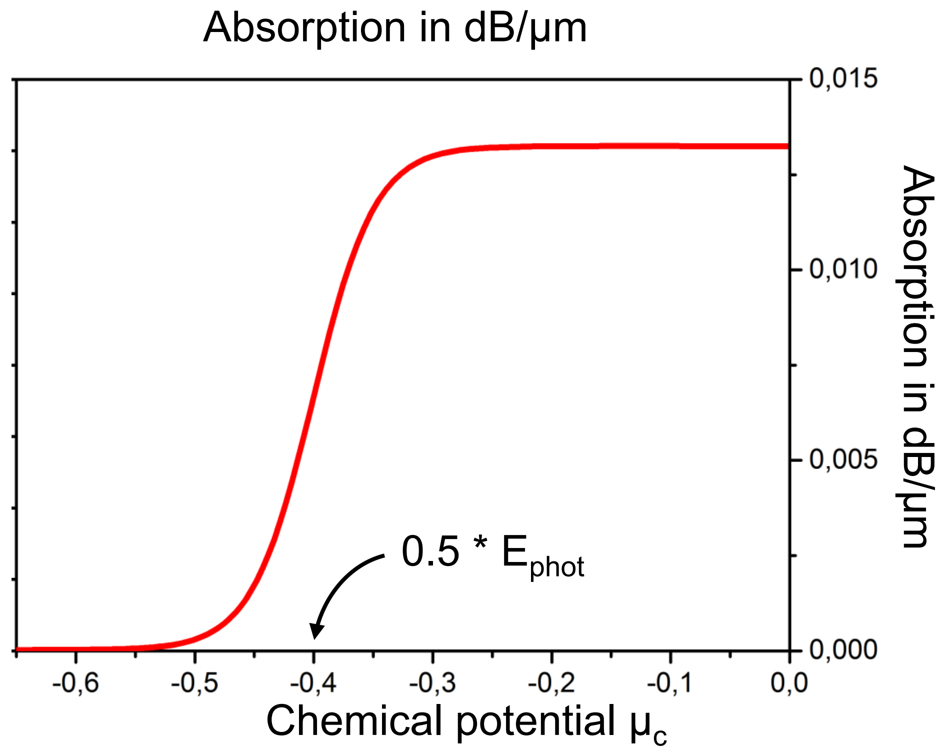


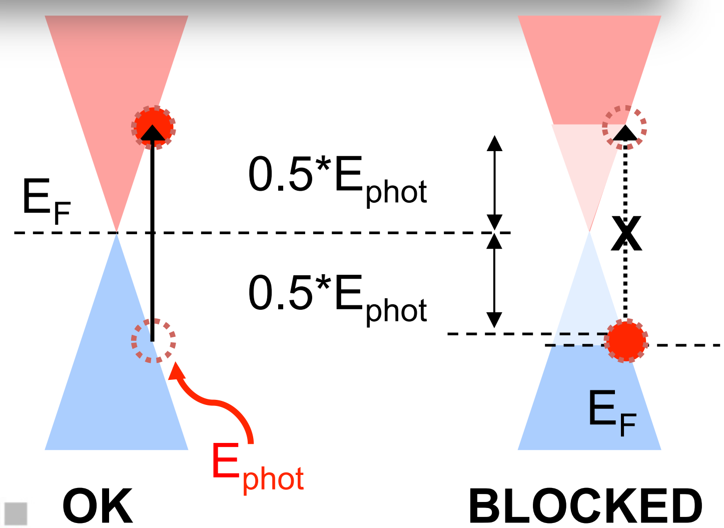
Schneider *et al.*, Nanoscale, 2017

Graphene / Silicon Photonics Integration

Simulation: absorption in graphene on Si waveguide







λ = 1550 nm → E_{phot} = 0.8 eV

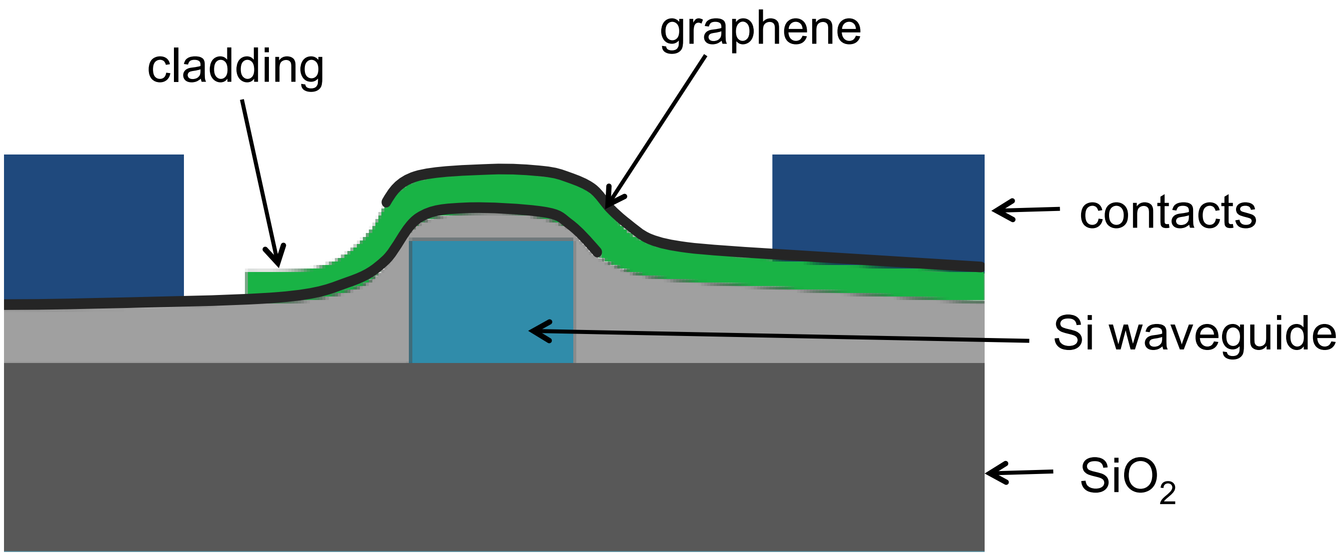
For $|\mu_c| \geq 0.5 * E_{phot}$ states are blocked

→ graphene becomes transparent

Kramers-Kronig enables phase modulation

Graphene / Silicon Photonics Integration

Absorption modulator

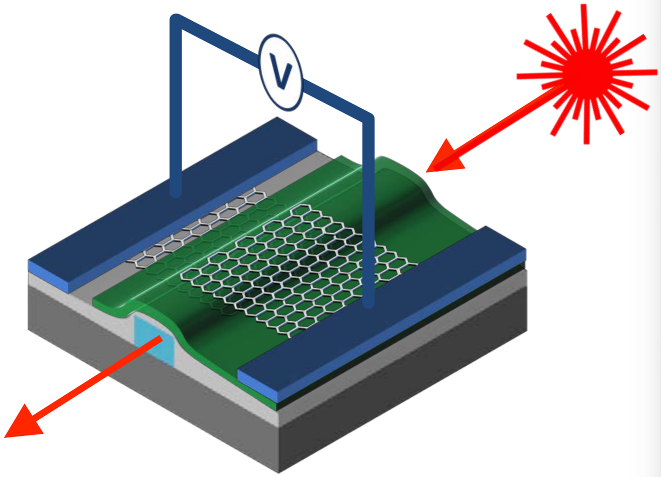


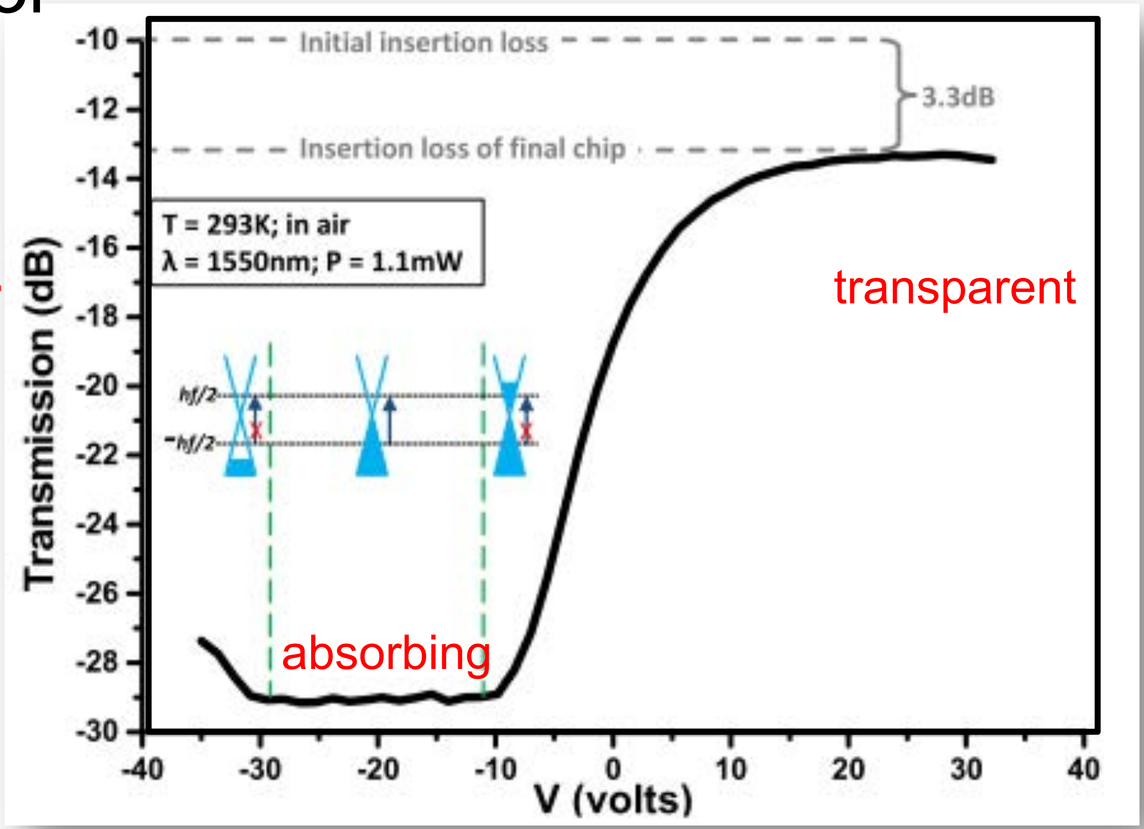
- SOI substrate 220 nm top Si
- Bottom electrode close to the waveguide surface
- Top electrode located in a distance of ~ 90 nm
- The lower electrode is adjusted between transparent and absorbing state

Mohsin et al. Optics Express 22, 15292 (2014)

Graphene / Silicon Photonics Integration

Absorption modulator





Mohsin et al. Optics Express 22, 15292 (2014)

High modulation depth, low insertion loss

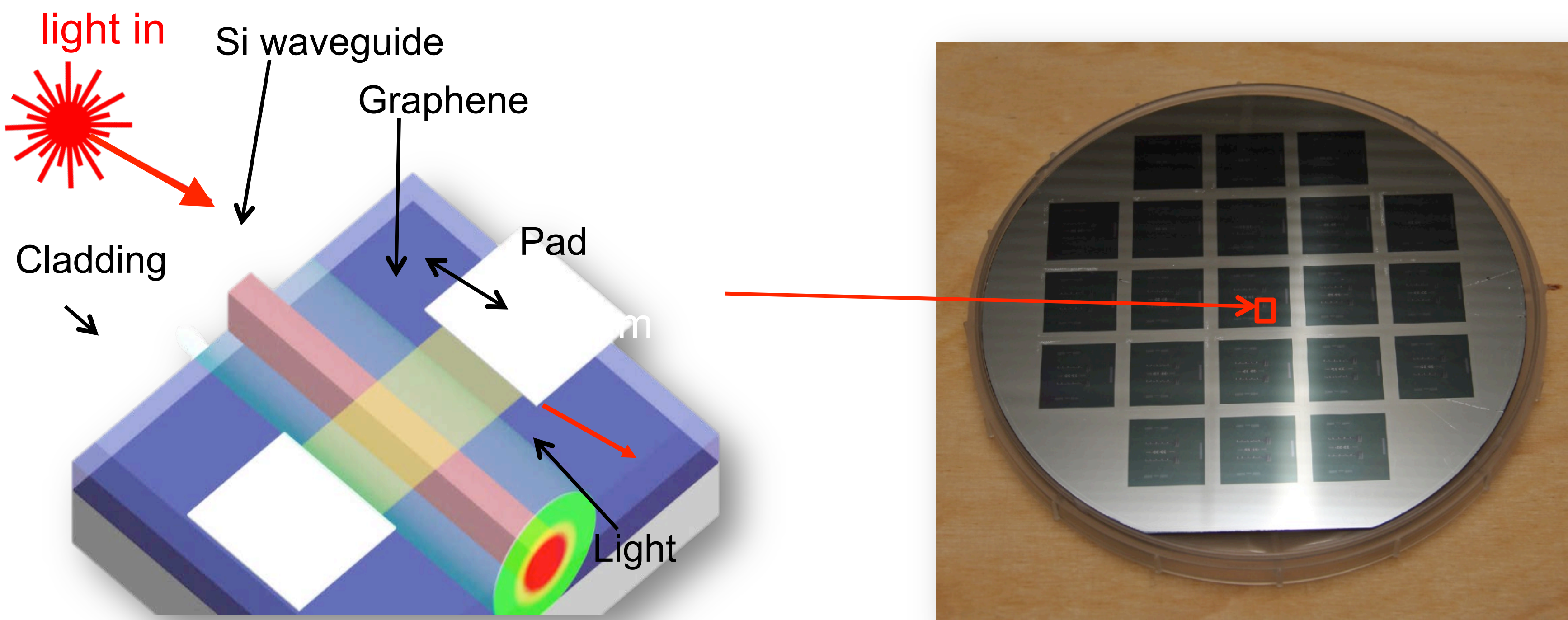
Graphene / Silicon Photonics Integration

Absorption modulator SOTA

Type	Moduation (dB)	Attenuation (dB)	Modulation/ Attenuation	Length (µm)	Bandwidth (GHz)
Graphene [1]	**16**	3	**5**	300	3,4
Graphene Simulation	16	<1	>15	<15	>50
Ge on Si [2]	6	6	1,2	30	40
Si [3]	5,5	4,2	1,3	5000	26,5

1) M. Mohsin et al. Optics Express 22, 15292 (2014)
2) D. Feng et al. Optics Express 20, 2224 (2013)
3) X. Tu et al. Optics Express 21, 12776 (2013)

Integrated graphene photodetector



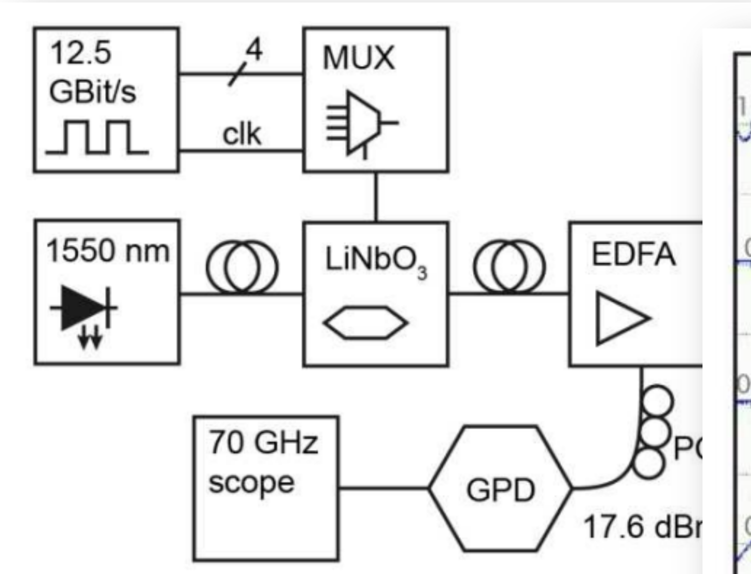
Graphene photodetector key merits:

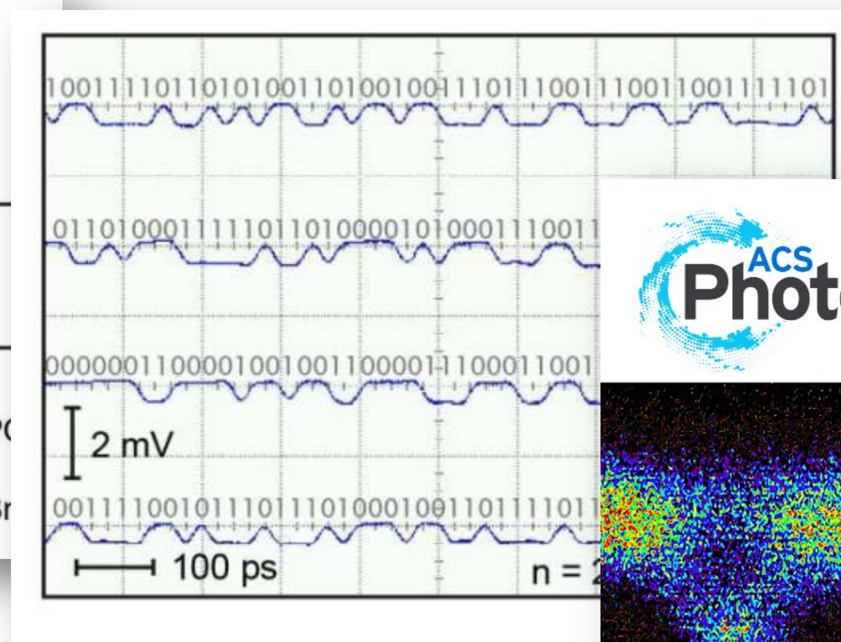
- Integrable on various substrates, here silicon (SOI) waveguide
- Possible intrinsic bandwidth: few hundred GHz
- **Ultrafast charge carrier dynamics ► ultrafast photonic devices**

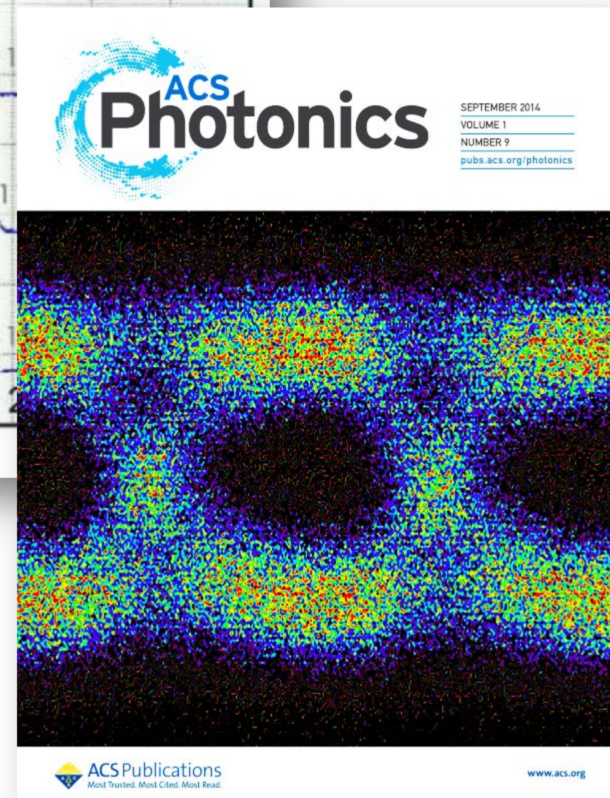
Graphene / Silicon Photonics Integration

Data transmission at 50 Gbit/s

D. Schall et al., ACS Photonics 1, 781(2014)



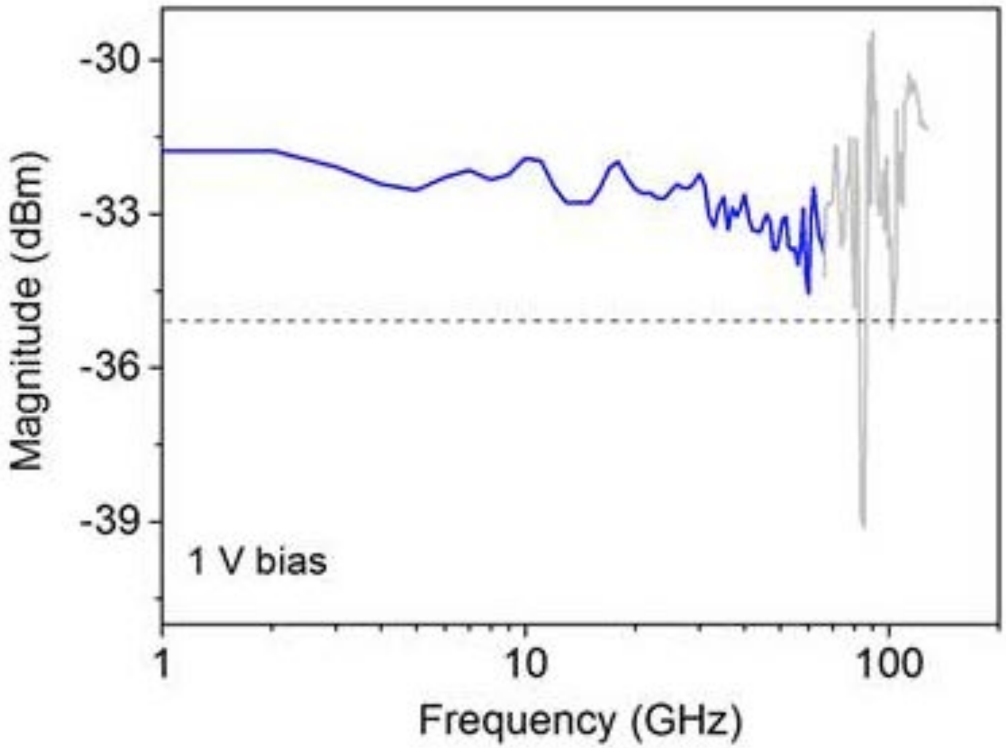




- 50 Gbit/s bit stream coupled to detector.
- Signal directly displayed at scope
- Excellent signal integrity
- System rise time 9 ps (bandwidth 40 GHz)
- Eye diagram for 1 channel at 12.5 GHz

RF response measured up to 130 GHz

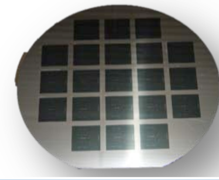
- RF signal through tunable heterodyne setup
- Measured with 67 GHz GS probes
  - Blue: calibrated up to 67 GHz
  - Grey: above min. expected losses at 67 GHz subtracted
- 1.85 mm cable and Bias Tee (calibrated up to 110 GHz)
- Power meter calibration factor determined up to 110 GHz

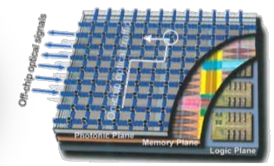


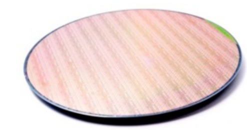
D. Schall et al., Optical Fiber Communication Conference, 2018

Graphene / Silicon Photonics Integration

Comparison: state of the art







	Graphene [1,8]	Graphene potential	Ge[2,4]
Max. Data Rate GBit/s	50 no bias > 180 calc	few 100 calculated[5,6]	40 no bias 56 bias
Max. Bandwidth GHz	**> 130**	> 200 [5,6]	120
Sensitivity A/W	**0.2**	0.4 .. 1 [7]	0.8 .. 0.9
Wafer-scale 3D integration	**Not perfect but fairly good**	**OK**	**NO only on Si**

Graphene integrated on non crystalline surfaces with very high performance

This is not possible with Ge!

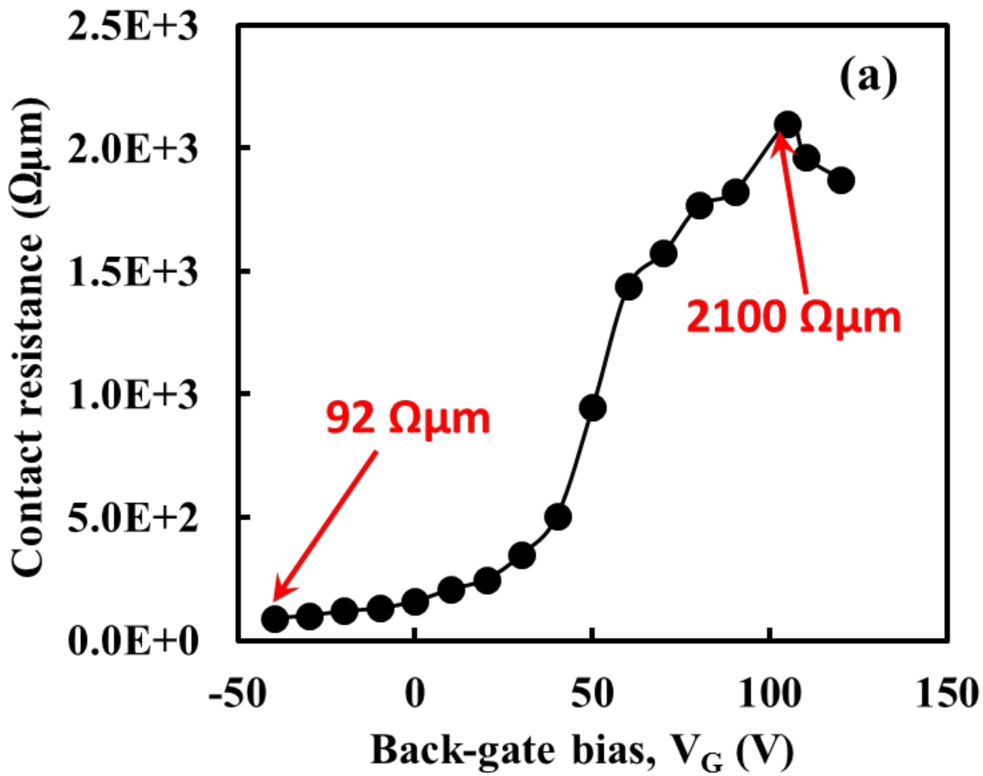
► Graphene candidate for 3D integration into „Photonic Super Chips“

1) Schall et al. ACS Photonics 1, 781 (2014)
2) Vivien et al. Optics Express 20, 1096 (2012)
3) Heinrich Hertz-Institute Berlin (2015)
4) Chen et al. Optics express 25, 5 (2016)
5) Urich et al. Nano Letters 11 (2007)
6) Tielrooij et al. Nature Nanotech 10 (2015)
7) Shiue et al. Nano Letters, 15 (2015)
8) Schall et al. J. Phys. D. (2017)

Integration Challenges: Electrical Contacts

Contact resistance

- Literature data is scattered
- Depends strongly on carrier density in Graphene
- ITRS specifications can be reached (< 50 Ωμm)
- There is no reproducible, reliable and manufacturable (i.e. standard) technology for electrical contacts



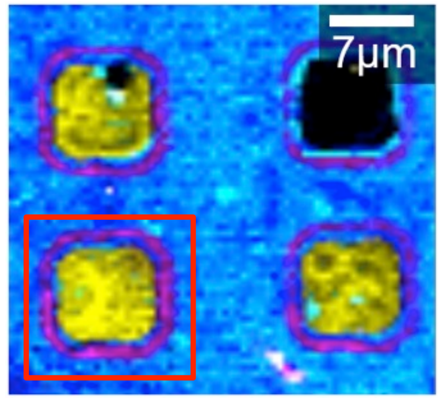
Cusati *et al*., IEDM, 2015
Gahoi *et al*., ESSDERC, 2016
Cusati *et al*., Sci. Rep., 2017
Passi *et al*., under review, 2018

Integration Challenges: Metrology

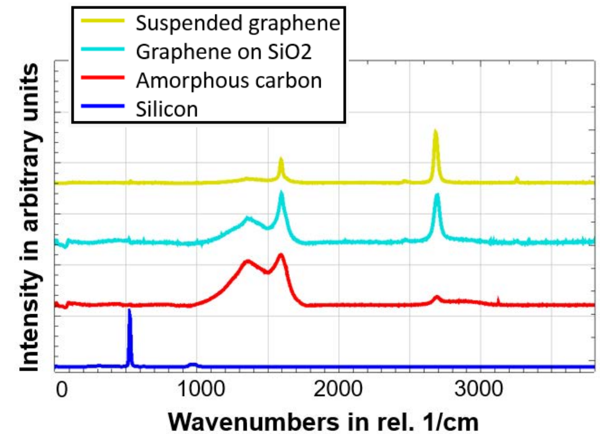
Raman Spectroscopy and Tomography

- Detection of intact graphene membranes
- Graphene property analysis:
  - Stress/strain
  - quality
  - defects,
  - doping
  - number of layers

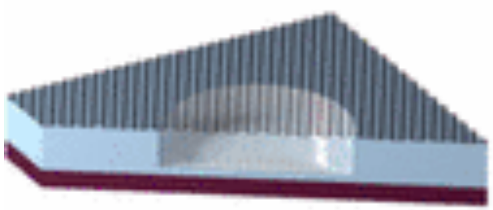
2D maps

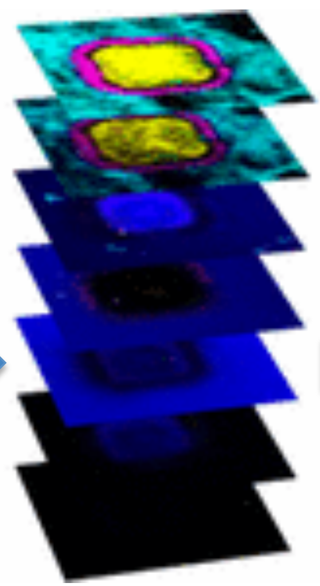


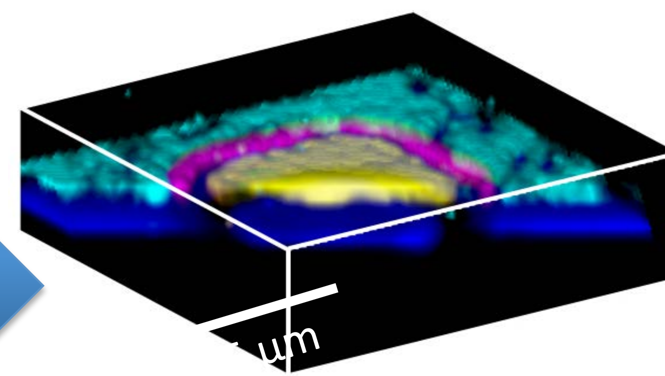
Extracted single spectrum



3D Raman Tomography





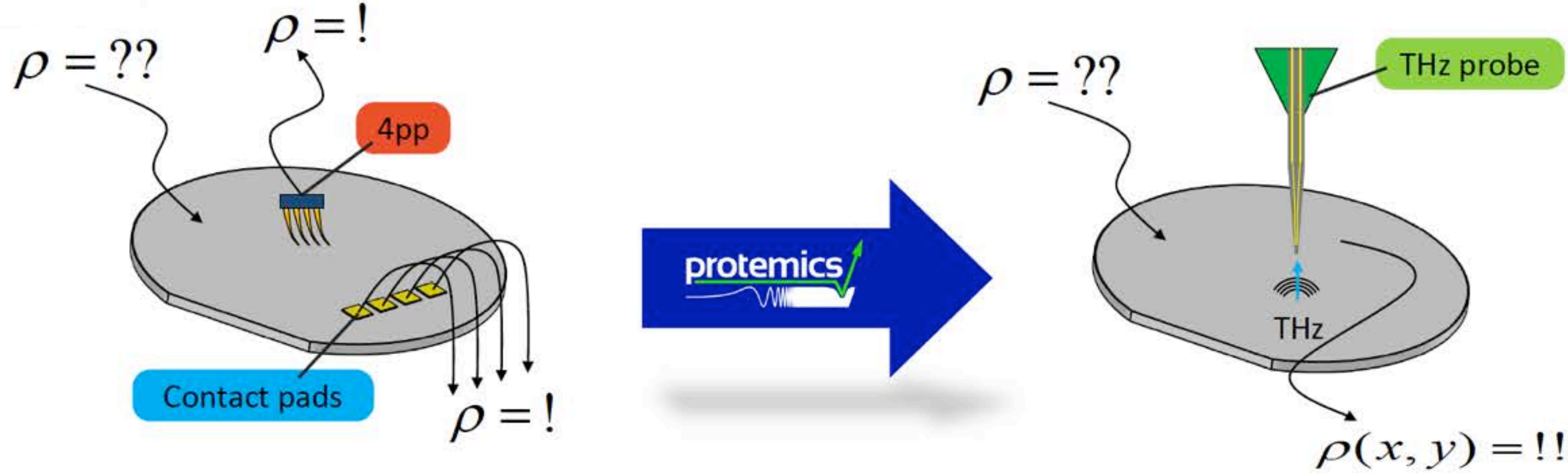


Wagner *et al*., Nano Letters, 2017

Integration Challenges: Metrology

THz near-field inspection

Protemics: spin-off from AMO



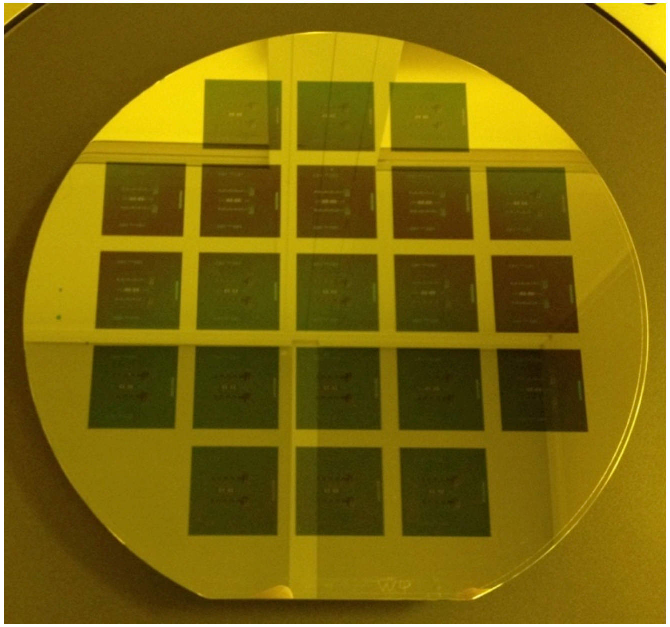
$\sigma = 1/\rho$
conductivity = 1/resistivity

Protemics' technology offers:

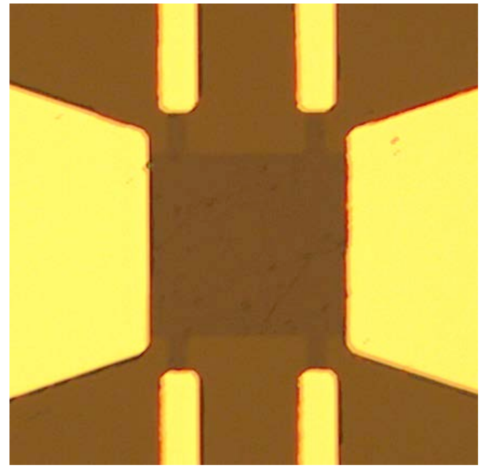
- **Much bigger insight** in material parameters than before. (R_s, N, n, t)
- **Non-contact** measurement technique
- **Full mapping** instead of point measurements due to fast, non-contact acquisition

Summary: Wafer-Scale Graphene Integration

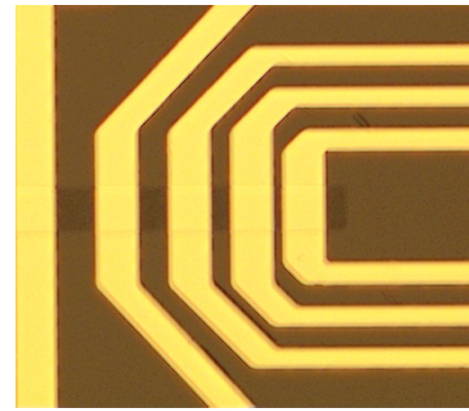
6-inch wafer



(Hall) Sensors

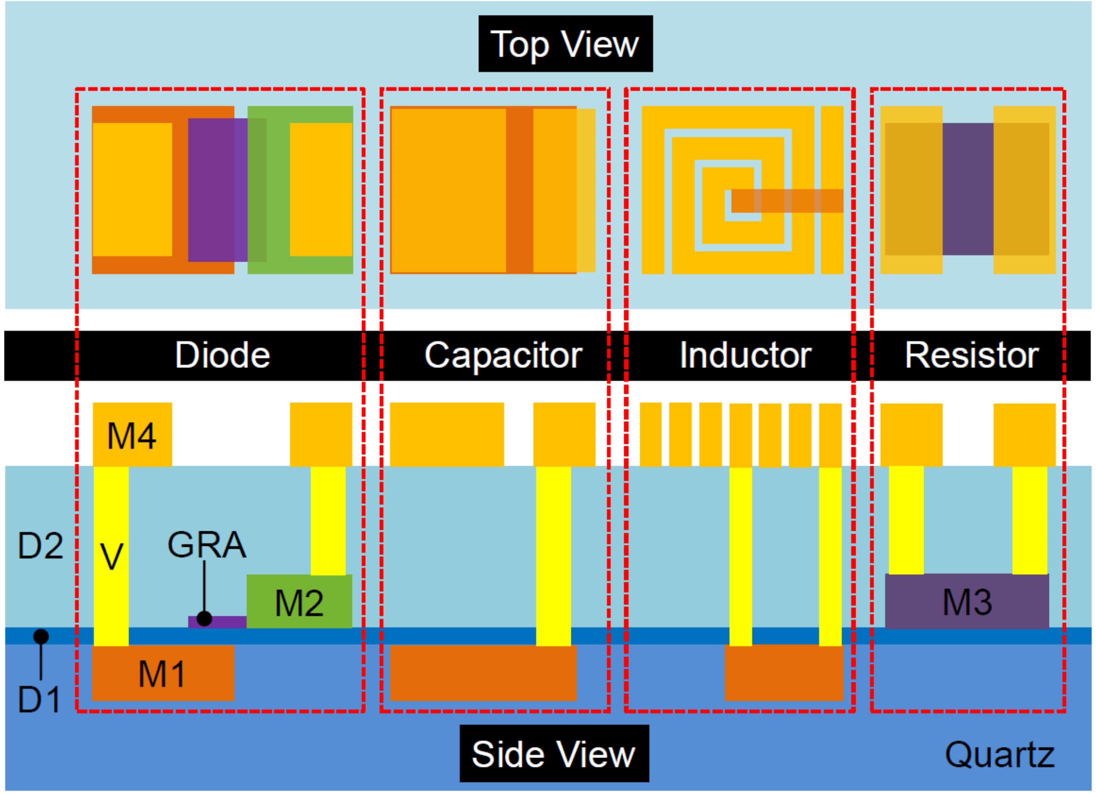


TLM structure



- 6 inch graphene grown and transferred by **Graphenea**
- Graphene devices fabricated by **AMO**
  - ➢ Semi-automated processing
  - ➢ High yield
  - ➢ Both standardized chips and customized processing possible
  - ➢ Contact: kleinjans@amo.de

Summary: MMIC process



Graphene is between D1 and M2, and can be used in diodes, varactors or/and transistors.

3 Dielectric layers:

- D1: 5 nm TiO2 (diodes)
  or 5-10 nm Al2O3 (FET)
- D2: 90nm Al2O3 (encapsulation, capacitors)
- D3 500 nm SU8 (inductors)

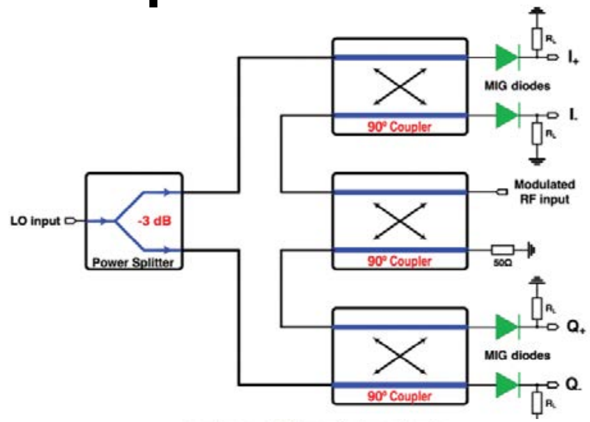
4 Metal layers:

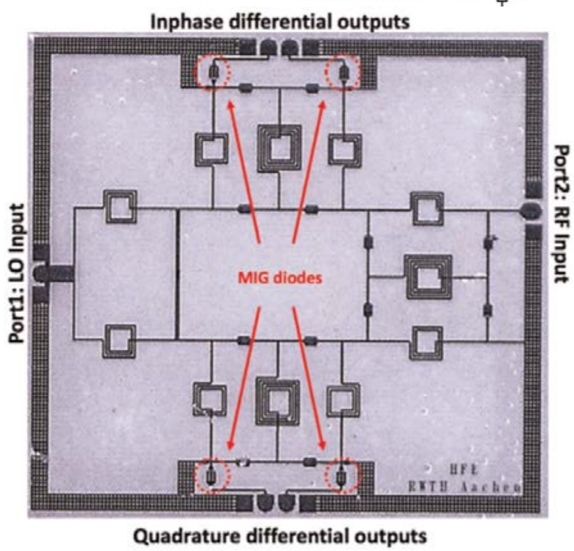
- M1: 100nm Al (gate electrode, passives)
- M2: 20 nm Nickel (graphene contacts)
- M3: 110 nm TiN (resistors)
- M4: 2µ Al (passives, interconnects)

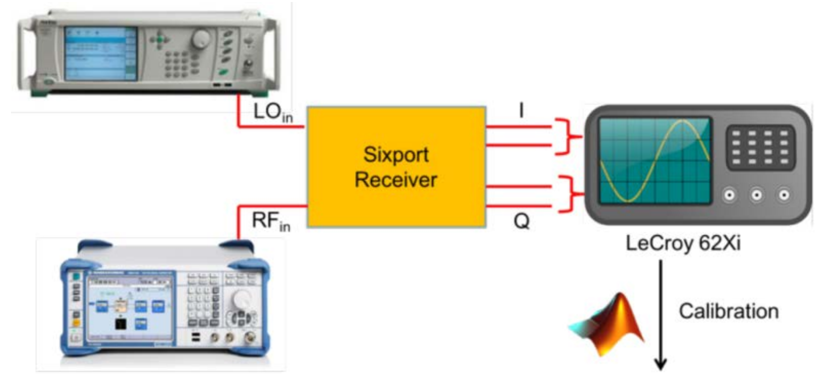
Saeed et al. Nanoscale, 2018, 10, 93

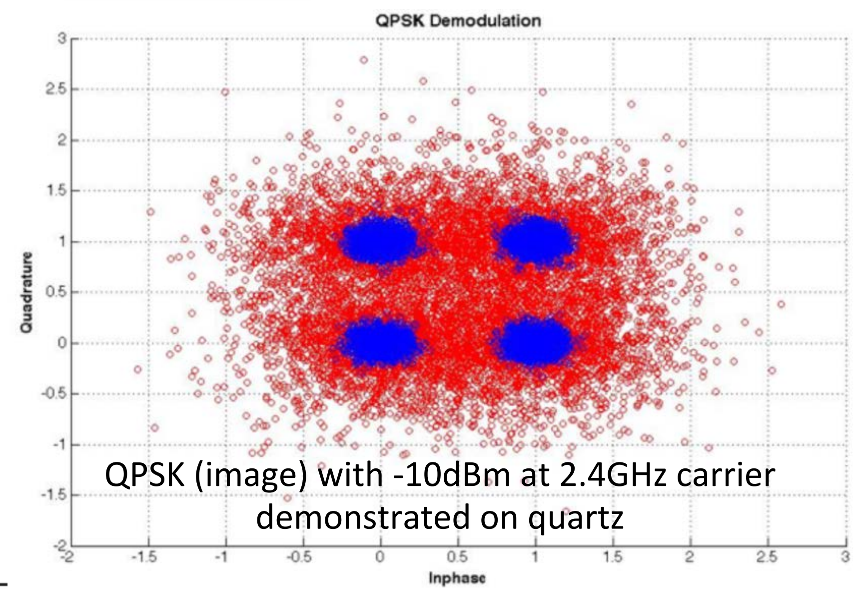
Summary: MMIC process

WiFi six-port receiver frontend on Quartz (Negra group, RWTH)









QPSK (image) with -10dBm at 2.4GHz carrier demonstrated on quartz

Scheme	No. of active devices	Modulation	f_{RF} (GHz)	P_{LO} (dBm)	Power consumption (mW)	Conversion gain (dB)
Single stage[28]	1 GFETs	Amplitude modulation	2.45	NA	NA	−35
Three stages[14]	3 GFETs	Frequency modulation	4.3	−2	20	−10
Six ports [This work]	4 MIG diodes	20 MHz QPSK	2.45	0	0	−7

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Summary: 2D R&D in Aachen

- CVD graphene and 2D materials device demonstration
- High performance devices:
  → NEMS: Pressure sensing, gas sensing (not shown)
  → RF Electronics: transistors & diodes (not shown)
  → Optoelectronics: diodes, absorption modulators, detectors, (heaters, attenuators, phase modulators)

- Integration issues: metrology, variability, reliability

- Wafer scale processing feasible

- System level demonstrators

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