

Device design parameters for carbon nanotube field-effect transistors

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Abstract

Among the extraordinary electrical characteristics, such as low scattering rate and high current-carrying capability, the intrinsic linearity of carbon nanotube (CNT) field effect transistors (CNTFETs) is expected to be beneficial for future high-frequency (HF) applications once the device is optimized [1], [2]. Performance projection studies [3] and fabricated proof-of-concept HF circuits [4]-[6] have shown the feasibility of CNTFETs for HF applications. Some technology related issues can be overcome by sophisticated techniques [7] and an adequate device characterization [8]. However, modeling and technology groups efforts are developed towards an optimized device suitable for mass production. An important performance parameter of the transport properties of the channel, such as the mobility, helps the device optimization. In addition, the metal-CNT interfaces, key factors limiting the device performance, need to be properly characterized by a Schottky barrier and a contact resistance in order to improve the current injection [9], [10]. A review on concepts and extraction methods of Schottky barrier height, contact resistance and mobility for carbon nanotube field-effect transistors (CNTFETs) is presented. The methods are applied to synthetic and experimental data of single- and multi-tube CNTFETs with short- and long-channel lengths obtained by our group [8], [11], [12].

References

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Figures

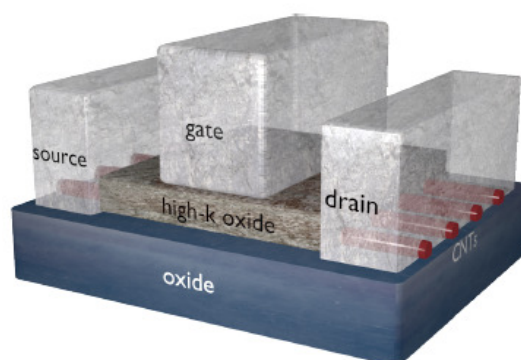


Figure 1: Top gate multitube CNTFET