Investigation of high frequency performance of hBN encapsulated Graphene Field-Effect Transistors

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Carrier mobility and saturation velocity in graphene are considerably enhanced when this two-dimensional material is encapsulated in hexagonal boron nitride (hBN) [1,2]. This work studies the theoretical limits of high frequency (HF) performance of hBN encapsulated graphene field-effect transistors (GFET). For such a purpose we have implemented a Monte Carlo simulator with the relevant scattering mechanisms, namely, carrier-carrier interaction, intrinsic phonons, remote surface polar phonons and scattering of carriers because of the presence of impurities and defects. Our simulator reproduces the experimental carrier mobility and saturation velocity dependence with carrier concentration [3]. This information is introduced in a self-consistent GFET drift-diffusion simulator that takes full account of short channel effects [4]. HF performance has been studied from a quasi-static small-signal charge-conserving model [5]. This way, direct current and HF are assessed. We have found that HF performance and device stability strongly depends on the bias point. Stability must be guaranteed in circuits targeting signal amplification. We have also observed that the GFETs are more prone to instability when they operate in the negative differential resistance. By using our drift-diffusion simulator, we have found that hBN encapsulated GFETs have the potential to work in the THz range for channel lengths below 200 nm. For comparison purposes we have plotted, in the same graph, the maximum oscillation frequency (f_{max}) that has been reported with Si and InP radiofrequency transistors. This work is funded by the European Union's Horizon 2020 research and innovation program (No 696656), the *Generalitat de Catalunya* (2014 SGR 384) and the *Ministerio de Economía y Competitividad* (TEC2015-67462-C2-1-R, MINECO/FEDER and FJCI-2014-19643).

References

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Figures

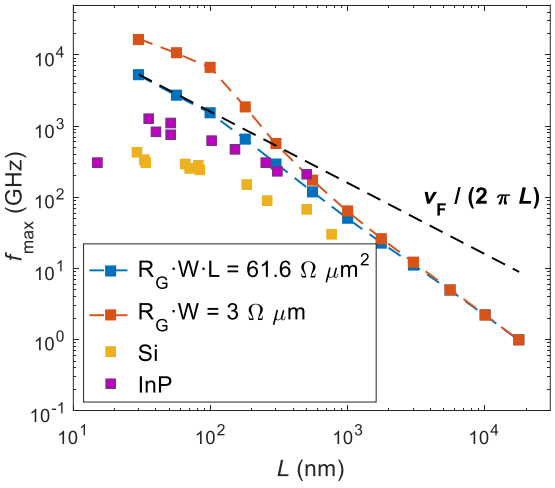

Figure 1: Scaling of simulated f_{max} of hBN encapsulated GFET at drain voltage V_{ds} = 0.1 V. Simulated performance has been benchmarked against state-of-the-art InP and Si technologies. Note that when gate resistance scaling assumption is applied (blue symbols) a sizeable f_{max} improvement is predicted.