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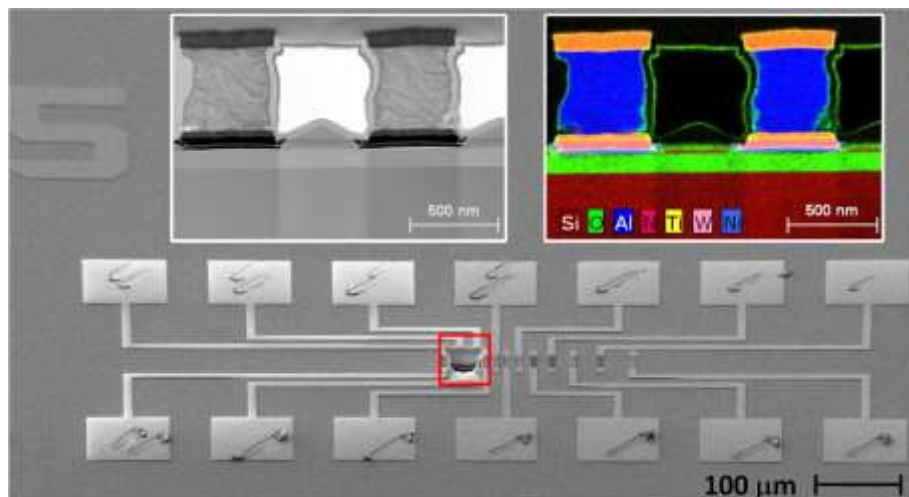
## Integration of graphene into 200 mm CMOS technology

Graphene has attracted a lot of attention for its unique physical properties [1,2]. The high electron mobility together with its two-dimensional structure makes it attractive for high speed electronic devices. Despite the significant progress in the fabrication of various graphene based microelectronic devices, the integration of graphene devices still lack the stability and compatibility with Si-technology processes. In this paper, we present the attempts to integrate graphene into the CMOS line, where several graphene concepts have been realized in 200mm silicon technology platform. We investigated different process module developments such as graphene synthesis on silicon compatible materials like germanium, a non-destructive deposition of dielectric materials on the graphene sheet as well as the combinations of these processes for various concepts of contacting on a full 200 mm wafers (Fig.1.)

### References

- [1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, A. A. Firsov, *Science* 306 (2004) 666.
- [2] A. K. Geim and K. S. Novoselov, *Nat. Mater.* 6 (2007) 183.

### Figures



**Figure 1:** Tilted SEM view of a TLM device with graphene. STEM (inset left) and EDX (inset right) analysis.