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Optimization of amorphous silicon deposition for fabrication of high-quality inverted graphene/silicon heterostructures

Introduction

Graphene is known as a material with exceptional electrical, mechanical as well as optical properties. It can be transferred to semiconducting materials, such as silicon, to form Schottky heterojunctions with the potential for producing low cost but very effective electronic devices, for example solar cells [1, 2] or photodetectors [3]. Graphene/silicon heterostructures are usually made of chemical vapour deposited (CVD) graphene transferred from metal catalyst (e. g., copper or nickel foil) to target substrate (e. g., silicon) by dry or wet transfer technique (stamping or fishing). Both transfer techniques use graphene-support polymers and are suitable for a high precision transfer of CVD graphene. However, they introduce substantial quantity of defects (graphene wrinkles, cracks) and impurities (from etchant or polymer residues) [4]. Therefore, these commonly used approaches are not suitable for fabrication of high-quality graphene/silicon heterostructures, especially not for large scale applications.

Here, we present an inverted approach to fabricate graphene/silicon heterostructures where hydrogenated amorphous silicon (a-Si:H) is grown on the top of 2D material by well-established plasma-enhanced chemical vapour deposition (PECVD). The first deposition of silicon film on the CVD graphene transferred to SiO_2/Si substrate has already been done by Arezki et al. [5]. In our study, to avoid the ill-defined interface and transfer-induced contamination, the a-Si:H films were deposited directly on top of CVD graphene covered copper foils. We aim to investigate a wide range of PECVD deposition temperatures (from room temperature to 350 °C) to find a compromise between minimizing the damage in graphene and maintaining, in the same time, electrical conductivity of a-Si.

Methods

Intrinsic a-Si:H films with a thickness of roughly 20 nm were deposited in a capacitively coupled PECVD setup operated at 40 MHz. The substrates (CVD graphene on copper foil) were heated up to various temperatures (the range between 150 °C and 350 °C is discussed in this abstract) and exposed to a glow discharge in a mixture of SiH_4 and H_2 with an RF power of 0.05 W cm^{-2} under a pressure of 70 Pa. Gas mixture ratios were set by gas flows: 8 sccm of SiH_4 and 40 sccm of H_2. To eliminate oxide contamination during the a-Si:H deposition, high purity silane (99.999%) and hydrogen (99.99999%) gases were used in a PECVD chamber with the base pressure of 10^{-5} Pa. The thickness of the silicon films was confirmed with Tencor Alpha–step 100 profilometer measurement of a step-edge made at a same time on a glass substrate.

Raman spectra were measured in a Renishaw Reflex setup using a 442 nm excitation He-Cd laser on a silicon/graphene/copper stack from the top side of a-Si:H. The wavelength of 442 nm is strongly absorbed in the silicon film; however, the film thickness of only 20 nm still allows measuring a graphene layer beneath it.

Experimental results and discussion

At first, the quality of graphene layer after the a-Si:H PECVD deposition was assessed by non-destructive Raman spectroscopy. Fig. 1(a) presents a Raman spectra series of CVD graphene capped by a-Si:H under PECVD temperatures ranging from 150°C to 250 °C. Interestingly, all samples show the G and 2D peaks characteristic for graphene monolayer indicating that the PECVD silicon deposition is not destructive for

graphene in general. However, from the absence of a D-band in spectra it is evident that the high structural quality of graphene monolayer was preserved only for the a-Si deposition up to 200 °C. Above this temperature, PECVD deposition causes graphene damage, as the D band starts to grow up.

Indeed, the electrical conductivity of intrinsic a-Si:H layers prepared by PECVD under selected temperatures on glass substrate was measured. As can be seen from Fig. 1(b), the measurement of a-Si:H prepared at 150 °C is very similar to 250 °C and has one order of magnitude lower conductivity than materials prepared at 300 °C and 350 °C. The slope of lines was used to calculate activation energy. Its values are gradually decreasing with the temperature increasing from 150 °C to 350 °C (0.67 eV, 0.64 eV, 0.60 eV, 0.58 eV, respectively) which proves that the electrical quality of silicon is getting worse. To sum up, we observed the electrical conductivity optimum for a-Si:H PECVD deposition at 150 °C.

Conclusion

Since the 'standard' configuration of graphene/silicon heterostructure with graphene transferred on top of silicon suffers from transfer-induced defects and contamination, the inverted structure with silicon deposited on graphene still on the copper foil has a great potential to avoid these pitfalls. We found compromise temperature of a-Si:H PECVD deposition on graphene at 150 °C, enabling us to produce high quality inverted graphene/silicon heterostructure with minimized graphene damage. At the same time, the a-Si layer has the best electrical conductivity. Next, we will try to solve another issue which is the removal of copper without damaging the graphene and not breaking the stack due to stress release. To conclude, we demonstrated that a-Si:H deposition by PECVD is a viable method for fabrication of inverted graphene/silicon heterostructure and would be valuable not only for potential solar cells but in the 'silicon' industry in general.

References

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Figures

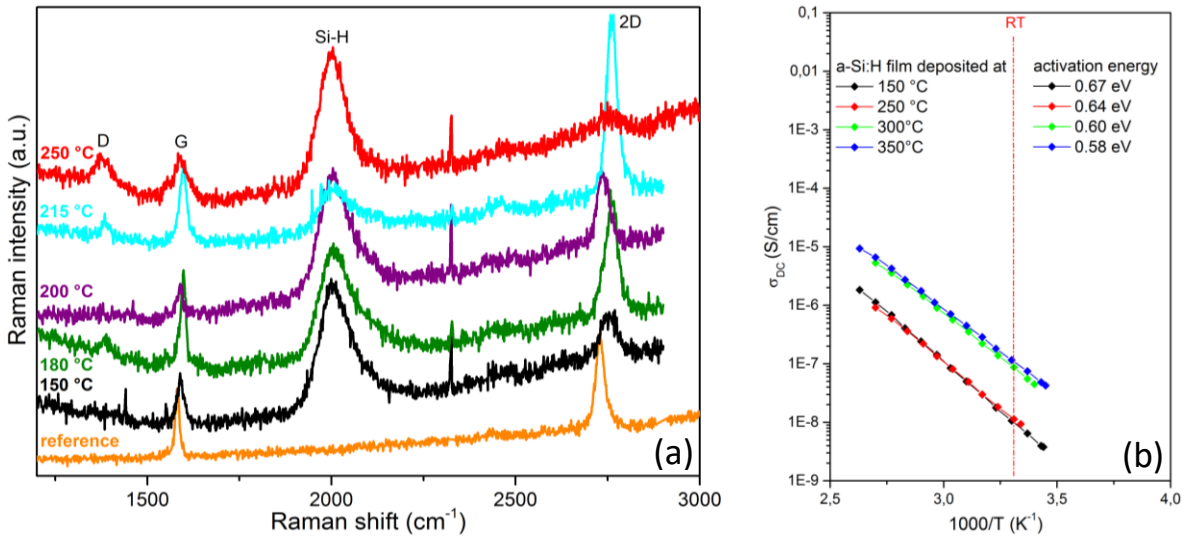

Figure 1: Characterization of a-Si:H/graphene inverted heterostructures prepared by PECVD under various temperatures. (a) Raman spectroscopy of CVD graphene covered by 20 nm of a-Si:H. (b) Results of a-Si:H electrical conductivity measurements.

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