A Manufacturable Pathway for Integrating 2D Materials into Advanced Semiconductor Process Flows

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The rapid scaling of next-generation electronic and photonic systems increasingly depends on the availability of high-quality, wafer-scale 2D materials that can be integrated within existing semiconductor process flows. In this talk, we present our latest advances in the synthesis and metrology of wafer-scale 2D materials—including graphene, MoS_2, WS_2, and h-BN—engineered for compatibility with front-end and back-end CMOS environments.

Our platform leverages optimized CVD growth, contamination-controlled transfer processes, and automated wafer-level characterization to deliver uniformity metrics suitable for device-grade manufacturing. We discuss key process parameters influencing grain size, defect density, epitaxy relationship, as well as strategies for mitigating common integration challenges.

We further demonstrate application-driven results across multiple device classes, including high-mobility FETs and heterogeneous 3D integration schemes. By combining materials engineering, scalable process design, and in-line metrology, our 2D wafer-scale platform provides a manufacturable pathway for incorporating atomically thin materials into advanced logic, sensing, and packaging architectures. This talk outlines both the current capabilities and the roadmap required to transition 2D materials from research prototypes to production-ready technologies.

Figures

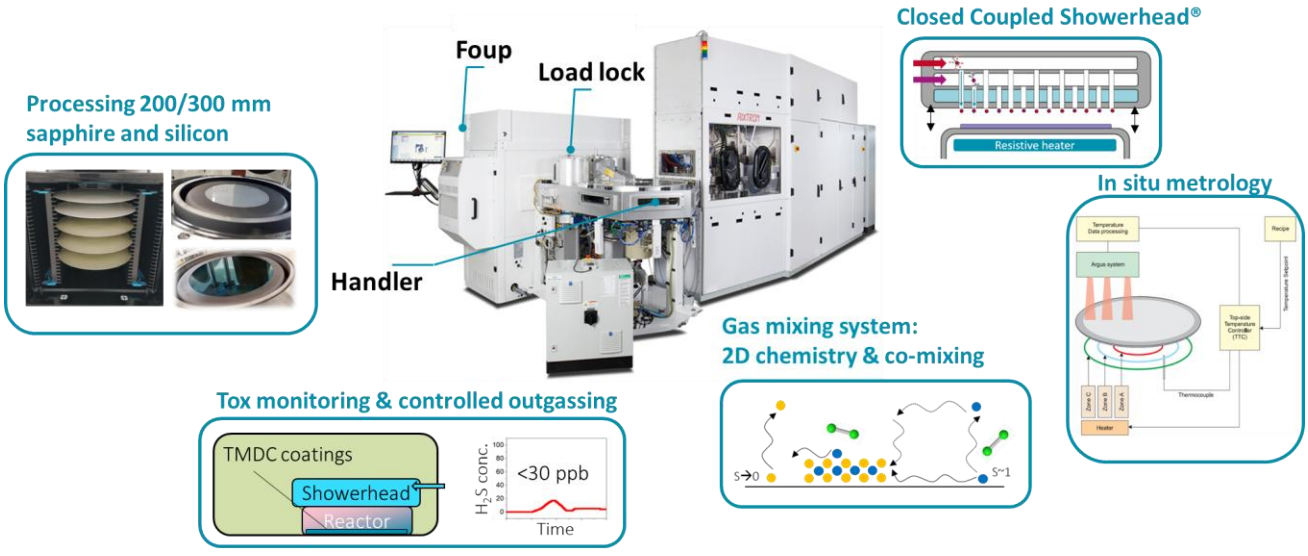

Figure 1: Photograph of an AIXTRON 300 mm MOCVD system for 2D materials, featuring automated load/unload transfer and capable of processing both 200 mm and 300 mm silicon and sapphire wafers. The options that enable seamless transfer of 2D material growth into a FAB production line are highlighted.